Dear Jeremy and others:

This is a report on room-temperature results of the first set of wafers that Jeremy sent to us for testing.

1 Summary of Results

In general, they look quite promising. The positive aspects of the data include:

1. Except where noted below, the leakage is typically below a few hundred fA.

2. The devices have good modulation, when acting as MOSFETs. For the devices with upper gates, $I_{\text{on}}/I_{\text{off}} \approx 10^6$ for the upper gate, and$I_{\text{on}}/I_{\text{off}} \approx 10^4$ for the lower gates.

The problems with these devices include:

1. In the 3G devices, the lower gates are typically all shorted to each other. We believe this problem has a simple solution: to stagger the lower gates geometrically.

2. Two out of the 4 SD-EL devices had leakage or were shorted between lower gates, upper gate, and the channel. On the other hand, two of the devices looked just fine. (It may be that the problematic leakages are parallel paths to back gate).

3. The most troubling problem: the back gate seems to be shorted to many of the leads (S, D, UG, LG-x) on the top of the chip. Also, after increasing the voltage on the back gates, this shorting problem seems to get worse. We believe that this also has a simple explanation: the BOX was etched away in the overlap regions.

The first page after the text has a handwritten summary of the devices. The first four columns denote whether or not the source current I_S equals the drain current I_D; this test shows whether or not there is leakage to the channel. The next column, "BG", denotes leakage to the back gate BG. The next four columns denote leakage to the upper gate "UG", and to the three lower gates, "LGD", "LGC", "LGS". The last four columns, "control", indicate the ability of the four gates to control the current, in terms of I_{on}/I_{off}.

2 Definitions

The next page has the overall layout of the wafer, with 30 dies. Please note that row 6 has a bunch of diagnostic devices; for the other five rows, all five columns are nominally identical. The dies are numbered left to right in each column, and then from top to bottom. For instance, row three column 1 is die number 11. We will concentrate on rows 3,4 and 5, which have in common the standard three gate device 3G, the attempt at a high temperature device HT, and the shuttle device SD part of which is another 3G. Going from row 3 to row 4 to row 5, in the 3G and the SD-EL devices, the fabrication pitch (width of lower gates, spacing between lower gates) gets larger so the devices

should get more reliable.

The next 3 pages have simple schematics of the layouts in rows 3,4, and 5. These won't give you all of the details, but should allow you to get the general idea of the layout for each row.

3 Electrical Results - Devices with UG

3.1 Die 17 device 3G

This device is from row four; the next page shows a micrograph of the devices on die 16 (in the same nominally identical row) with etched crystalline Si channel and poly-Si lower gates. The upper gate was put on later.

The next page shows a measurement of the device as a function of the upper gate voltage. Please see the page following this for the values of the parameters used. Note that the data file name is "Aug3_10"; this name can be found above the top of the graph, and is also used to define the values of the parameters. The measurement system defines current to be positive if it is flowing into the device, and negative if it is flowing from the device back into the measurement system. In order to plot things on a logarithmic vertical scale, I have taken the absolute value of all currents.

Please note the following:

1. The noise floor of the measurement system is a few tens of fA.

2. The source current and the drain current are equal; this indicates no leakage to the channel.

3. The upper gate and the lower gate nearest to the drain LG-D both have quite small currents, less than about 100 fA, over most of the range.

4. The upper gate controls the current quite well, with a ratio $I_{\rm on}/I_{\rm off} \approx 10^6$.

The next three pages, Aug3_20, Aug3_21, Aug3_22, show the dependence of the currents on all three of the lower gates. In general, the lower gates also control the current in the channel, although with a weaker dependence. Note that the current through two of the three lower gates is very high; this is because those two lower gates are shorted together. The next page shows a compilation of the dependence of the drain current on each of the three lower gates; the dependence is quite similar for all three. Note however, that to some extent this is not showing only the uniformity of the gates, because two of the gates are shorted together. However, in general the effect of the lower gates was quite homogeneous for all devices, including ones where the lower gates were not shorted together.

3.2 Die 17 device SD-EL

This device is the one entitled "SD2 top" in the micrograph. The next page shows Aug4_5, which shows the dependence on the upper gate; again, please refer back to the Table for voltage parameters.

The next page shows Aug4_13, which shows the dependence on lower gate LG-D. Again, the control of the channel current by the lower gate is quite good, similar to the 3G device. In contrast to the 3G device, the leakage from the lower gate is very low, below 100 fA except when $|V_{\rm LG\text{-}D} - V_{\rm UG}| > 5V$.

An obvious question is: why is the leakage in the SD device so much better than in the 3G? We believe that this is evident in the micrograph: for "3G40", the three lower gates all come from the same side; in other photographs not shown, it is clear that there is sometimes leftover poly-Si bridging between three gates with a similar geometry. In contrast, for "SD2 top", the three lower gates are staggered; in all staggered geometries, we have seen good isolation in the micrographs between the lower gates. Thus, we intend to stagger lower gates for all devices in the future.

3.3 Die 23 device HT

In general, I had quite a difficult time getting the HT device to function. This is because the HT device does not have an upper gate, and so in order to turn it on, we have to use the back gate. In general, I found the back gate was shorted or leaked to many of the other pins on the die. For the HT device, see the micrograph on the next page.

However, I was able to use the back gate effectively, and thus to get the HT device to function, by unshorting all of the other pins on the die. The next page, Aug19_40, shows the dependence on back gate voltage. The drain current shows reasonably good modulation by the back gate. In contrast, it is clear that the back gate is leaking to the source. The next page, Aug19_42, shows the dependence on one of the two lower gates, LG-D. Again, the drain current shows reasonable modulation by the lower gate.

3.4 Back gate leakage

In general, I found that the back gate was leaking or shorted to many of the pins on the die; currents ranged from pA up to tens of μA. The next page, Aug19_15, is from die 22 device HT. It shows that, with all pins unshorted except the three for which I was measuring the current, the total leakage out of the back gate over the range from -5 to +5 V was less than 10 pA. By repeatedly shorting and unshorting various pins, I determined that a single pin on the die, # 3, was the dominant connection to the back gate. With this pin shorted, the current out of the back gate ranged up to 10 μA; with this pin unshorted but 22 other pins on the die connected, the current was less than 30 pA over the range from -5 to +5 V.

This allowed me to test the back gate control of device 3G on this die; the back gate did indeed control the channel current. However, I then tested the back gate over a wider range from -10 to +10 V, at which point the back gate started leaking to other pins on the die!

I can sum up the observations about the back gate:

1. The back gate in general leaks to or is shorted to many of the pins connected to the devices on top of the die. The current ranges from pA up to tens of μA. Note that there is 200 nm of buried oxide in this SOI wafer; the wafer was produced by the thermal bonding technique, not the oxygen implantation technique.

2. With many other pins unshorted, if the leakage from the back gate is reduced to an acceptable level, the back gate can indeed modulate channel currents.

3. When I increased the range of back gate voltages, starting at [-5, +5] and ending at [-10, +10], new leakage paths were opened between the back gate and other pins on the top of the die.

4. The pins to which the back gate leaks are not consistent from one die to another; the placement and number of pins seems to be random, although I did not do a very comprehensive test of this.

4 Electrical Results - Device without UG

Some of the wafers did not have an upper gate layer deposited; the device ended with the lower gate and passivation oxide on the lower gates. I briefly tested a couple of items on one device, and saw that the general characteristics were identical with those in the wafer with an upper gate.

4.1 Die 18 device 3G

This device was similar to the one shown previously; in particular, the lower gates are indeed shorted together.

4.2 BG leakage

Again, the results are similar. The back gate is connected with what appears to be a random distribution to various pins on the top of the die. In particular, the next two sets of data (Aug22_20 and Aug22_18) illustrate the effect of just one pin: the first set of data has pin 9 shorted; there is a large current from BG, and the source-drain current does not look reasonable. The second

set of data has pin 9 unshorted; there is a much smaller current from BG, and the source-drain current is modulated by about one order of magnitude, and there does not appear to be any leakage to the channel.

When I repeated the first set of data, but with the wirebond connecting the post on the chip mount to the pad on the chip, I saw that the leakage from the back gate was much lower (less than 1 pA). This confirmed that the leakage is indeed within the device, and not through the chip mount.

$I_S = -I_D$

	UG	LGD	LGC	LGS
#17 BG	✓	✓	✓	✓
HT	no cond. (BG bad)			
SD-EL	✓	✓		✓
#20 BG	✓	✓	✓	✓
SD-EL	>10pA	>20pA		>100pA
#22 BG	✓	✓	✓	✓
SD-EL	✓	✓		✓
#23 BG	✓	~~>~~ 1pA (S)		
SD-EL	>10pA	>2pA		
HT	$I_D = -I_S > 100pA$			

BG leak

	UG	LGD	LGC	LGS
	<100fA	short I_{SD} <100fA		<300fA
	<300fA	to UG 10pA, $V_{LGD} < -4.5V$		same
	1nA	shorted 4μA		4μA
BG 10μA/ DS UG <10pA	<100fA	all shorted V<0		
	<100fA	all 3 > 100nA shorted		
	<100fA	<100fA $V_{LGD} > -4V$		<100fA $V_{LGC} > -4.5$
<30pA except pins	300fA	shorted		
	1nA!	1nA		

BG shorted to S

	UG	LGD	LGC	LGS
	10^6	1000	~~>~~300	2×10^3
	~~3×10^6~~	~~10^4~~		
	3×10^6	10^4		10^4
	10^5	3000	300	1000
	10^3	10		10
	2×10^5	10^4	10^4	10^4
	10^6	2×10^4		~~6000~~ ~~3000~~
	10^6	10^4		
	3×10^6	10^5		

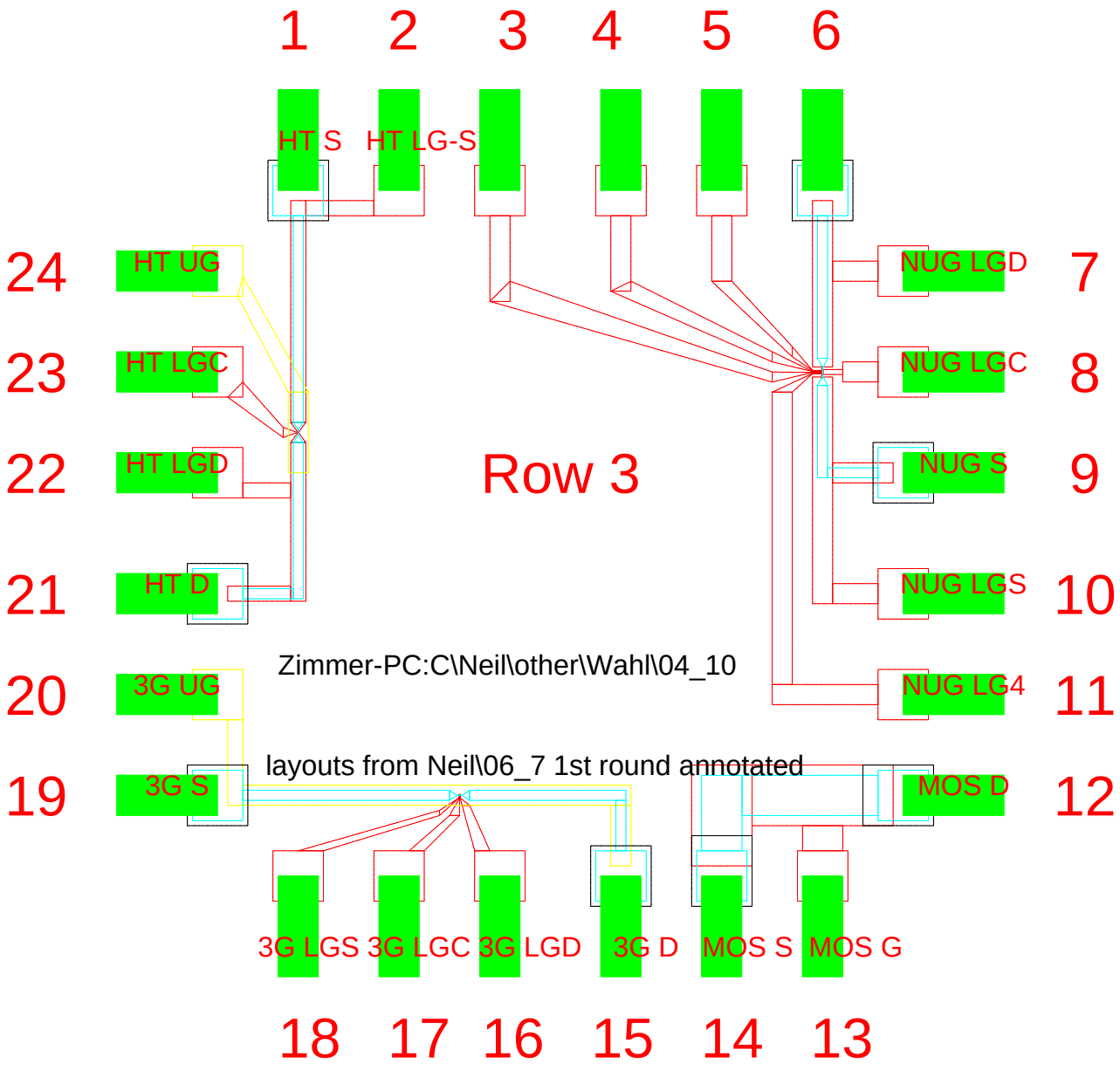
I_D exponential 10^5

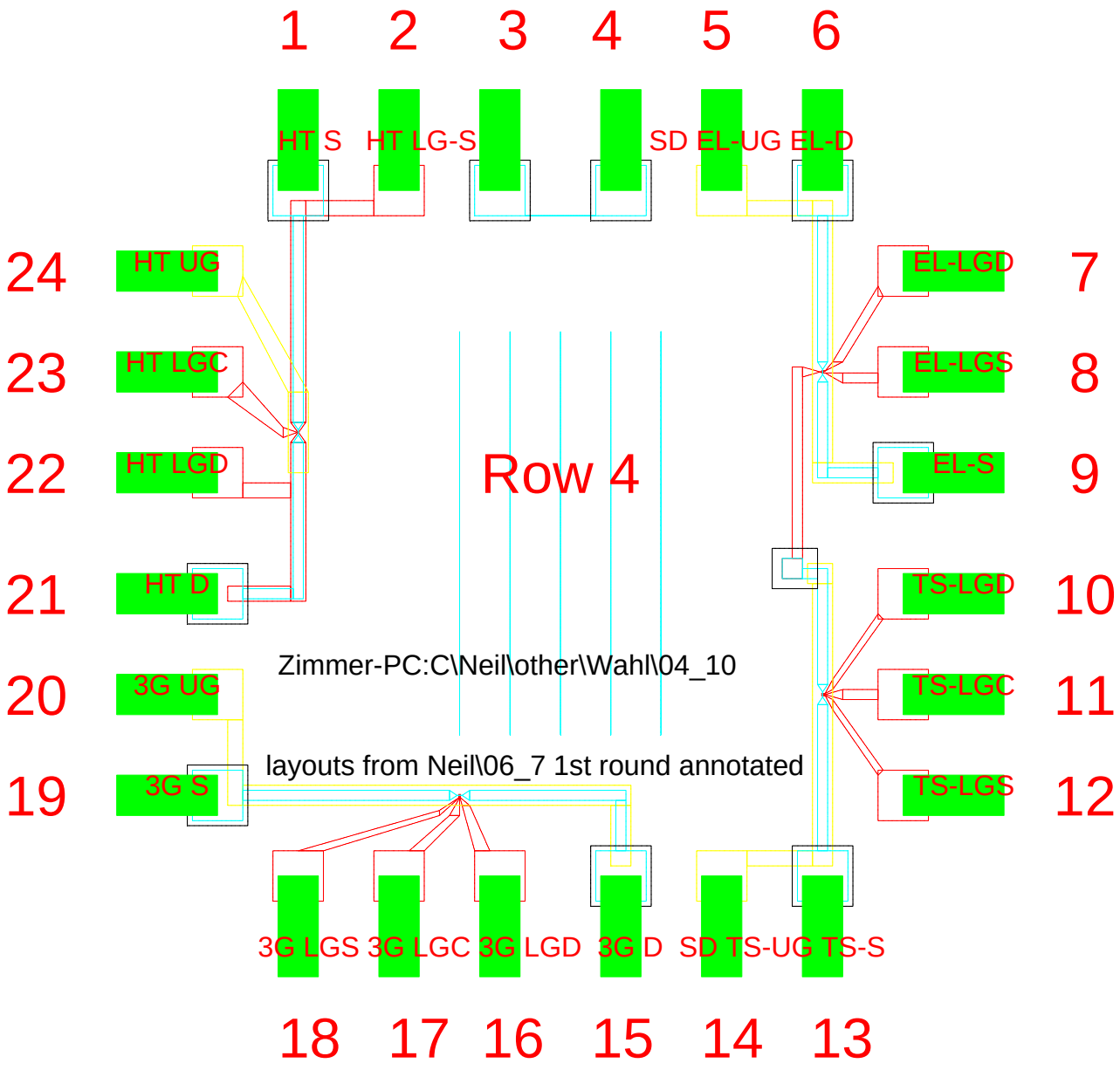
LG-D shorted to S!!

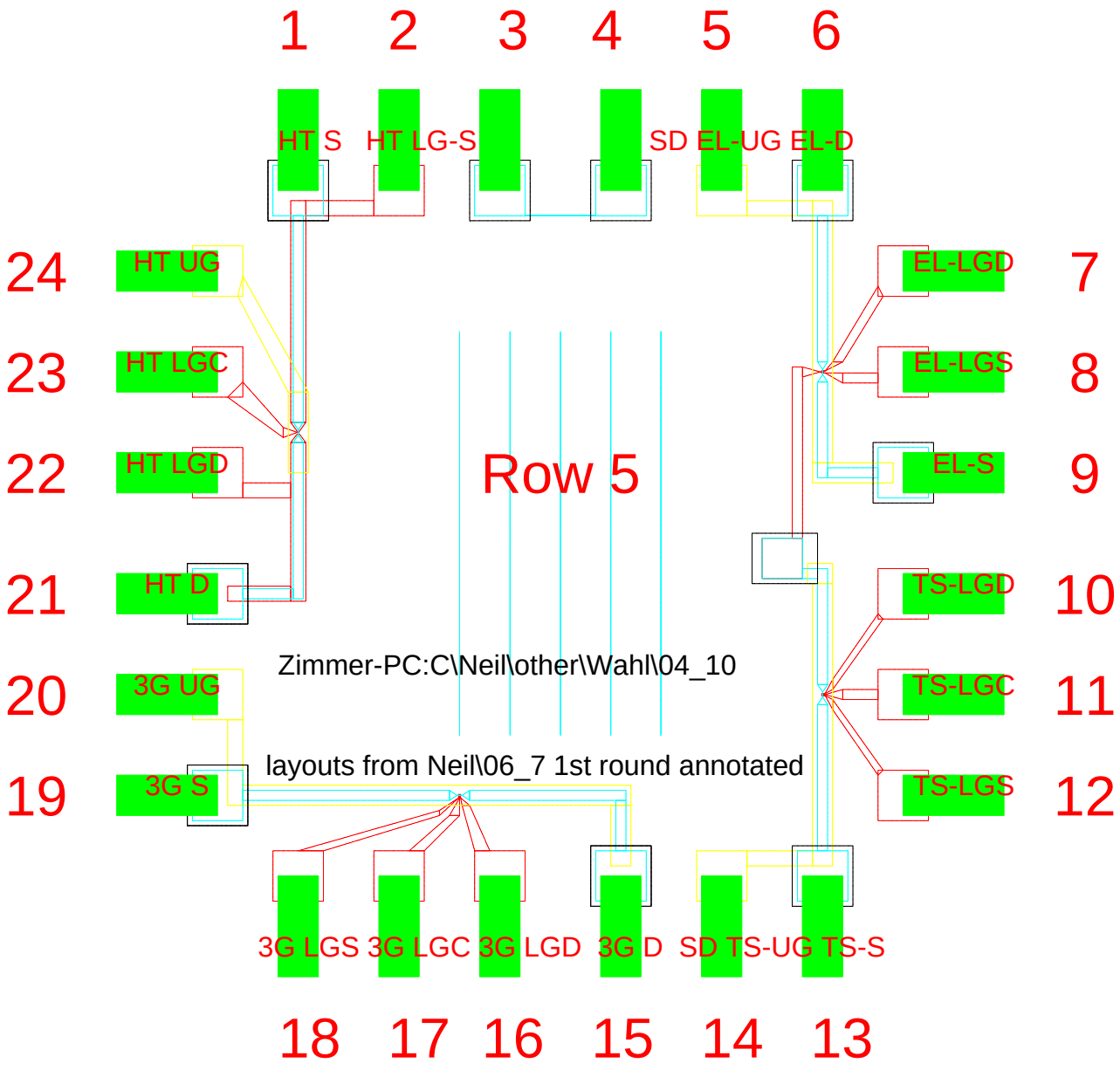
Die allotment (from Neil 4/06)

	1	2	3	4	5
1	2 X NUG2 SD-1	2 X NUG2 SD-1	2 X NUG2 SD-1	2 X NUG2 SD-1	2 X NUG2 SD-1
2	NUG3, HT, 3G, MOS-4	NUG3, HT, 3G, MOS-4	NUG3, HT, 3G, MOS-4	NUG3, HT, 3G, MOS-4	NUG3, HT, 3G, MOS-4
3	NUG4, HT, 3G, MOS-4	NUG4, HT, 3G, MOS-4	NUG4, HT, 3G, MOS-4	NUG4, HT, 3G, MOS-4	NUG4, HT, 3G, MOS-4
4	HT, 3G, SD-2, 1L-0	HT, 3G, SD-2, 1L-0	HT, 3G, SD-2, 1L-0	HT, 3G, SD-2, 1L-0	HT, 3G, SD-2, 1L-0
5	HT, 3G, SD-4, 1L-0.05	HT, 3G, SD-4, 1L-0.05	HT, 3G, SD-4, 1L-0.05	HT, 3G, SD-4, 1L-0.05	HT, 3G, SD-4, 1L-0.05
6	SD-8, 1DNG, 1D	SD-8, 1DNG, 1D	SD-8, cap	SD-8, cap-0.05	SD-8, cap-0.1

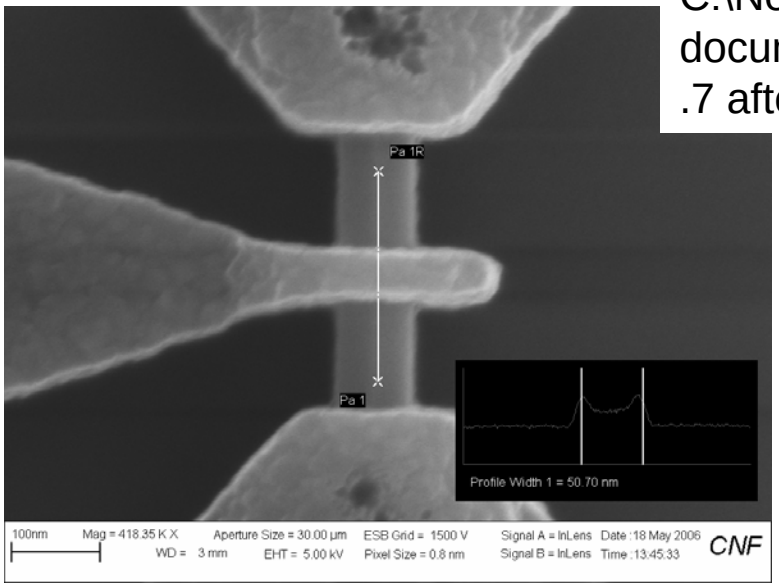
- No upper gate (NUG)
  - 10 2-fingers (NUG2),
  - 5 3-fingers (NUG3),
  - 5 4-fingers (NUG4)
- High temperature (HT)
  - 20 devices
- 3-gate SETT (3G)
  - 20 devices
- Shuttle Device (SD)
  - 20 devices
- 80 total devices


1
2
3
4
5
6
HT S
HT LG-S
24
HT UG
23
HT LGC
22
HT LGD
21
HT D
20
3G UG
19
3G S
NUG LGD
7
NUG LGC
8
NUG S
9
NUG LGS
10
NUG LG4
11
MOS D
12
Row 3
Zimmer-PC:C\Neil\other\Wahl\04_10
layouts from Neil\06_7 1st round annotated
3G LGS
3G LGC
3G LGD
3G D
MOS S
MOS G
18
17
16
15
14
13

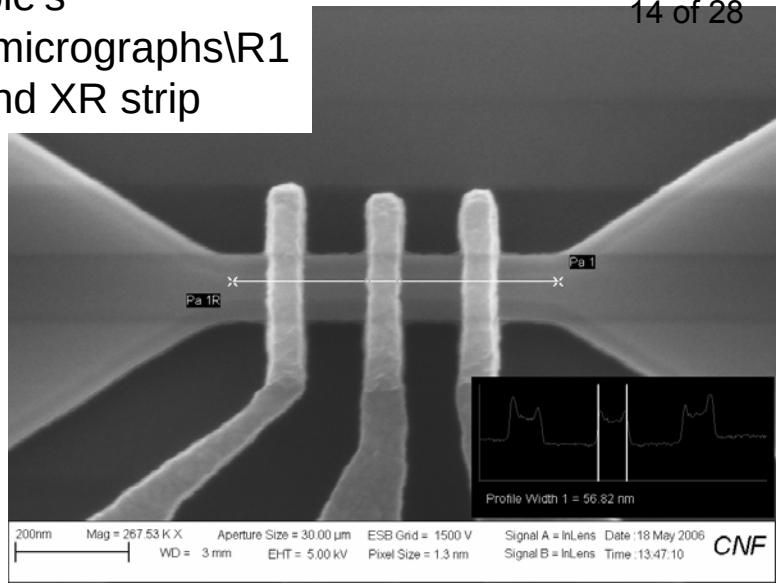

1
2
3
4
5
6
HT S
HT LG-S
SD
EL-UG
EL-D
24
HT UG
7
EL-LGD
23
HT LGC
8
EL-LGS
22
HT LGD
Row 4
EL-S
9
21
HT D
TS-LGD
10
Zimmer-PC:C\Neil\other\Wahl\04_10
20
3G UG
TS-LGC
11
layouts from Neil\06_7 1st round annotated
19
3G S
TS-LGS
12
3G LGS
3G LGC
3G LGD
3G D
SD
TS-UG
TS-S
18
17
16
15
14
13


1
2
3
4
5
6
HT S
HT LG-S
SD
EL-UG
EL-D
24
HT UG
7
EL-LGD
23
HT LGC
8
EL-LGS
22
HT LGD
Row 5
EL-S
9
21
HT D
TS-LGD
10
Zimmer-PC:C\Neil\other\Wahl\04_10
20
3G UG
TS-LGC
11
layouts from Neil\06_7 1st round annotated
19
3G S
TS-LGS
12
3G LGS
3G LGC
3G LGD
3G D
SD
TS-UG
TS-S
18
17
16
15
14
13

C:\Neil\other people's documents\Wahl\micrographs\R1.7 after LG etch and XR strip

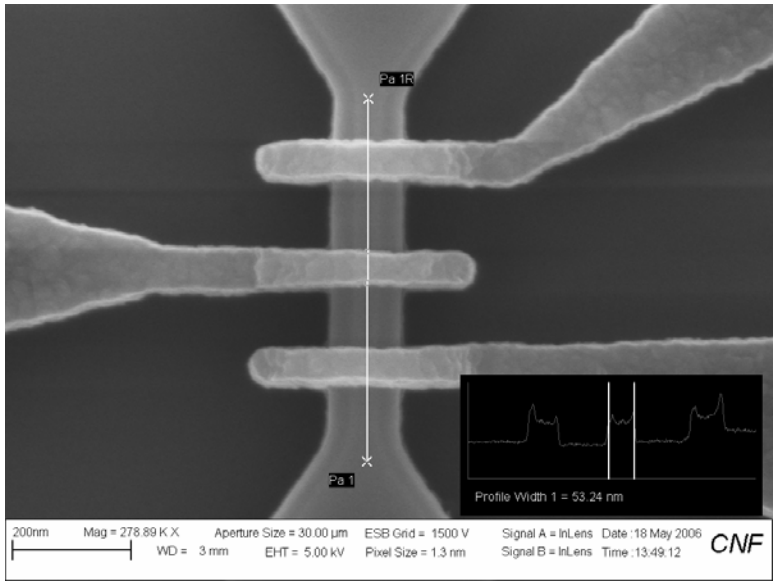


Die 16 HT40

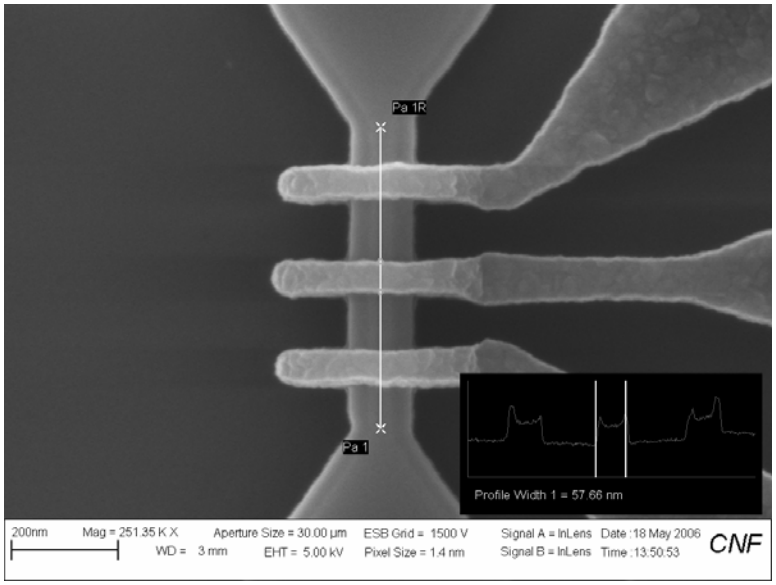


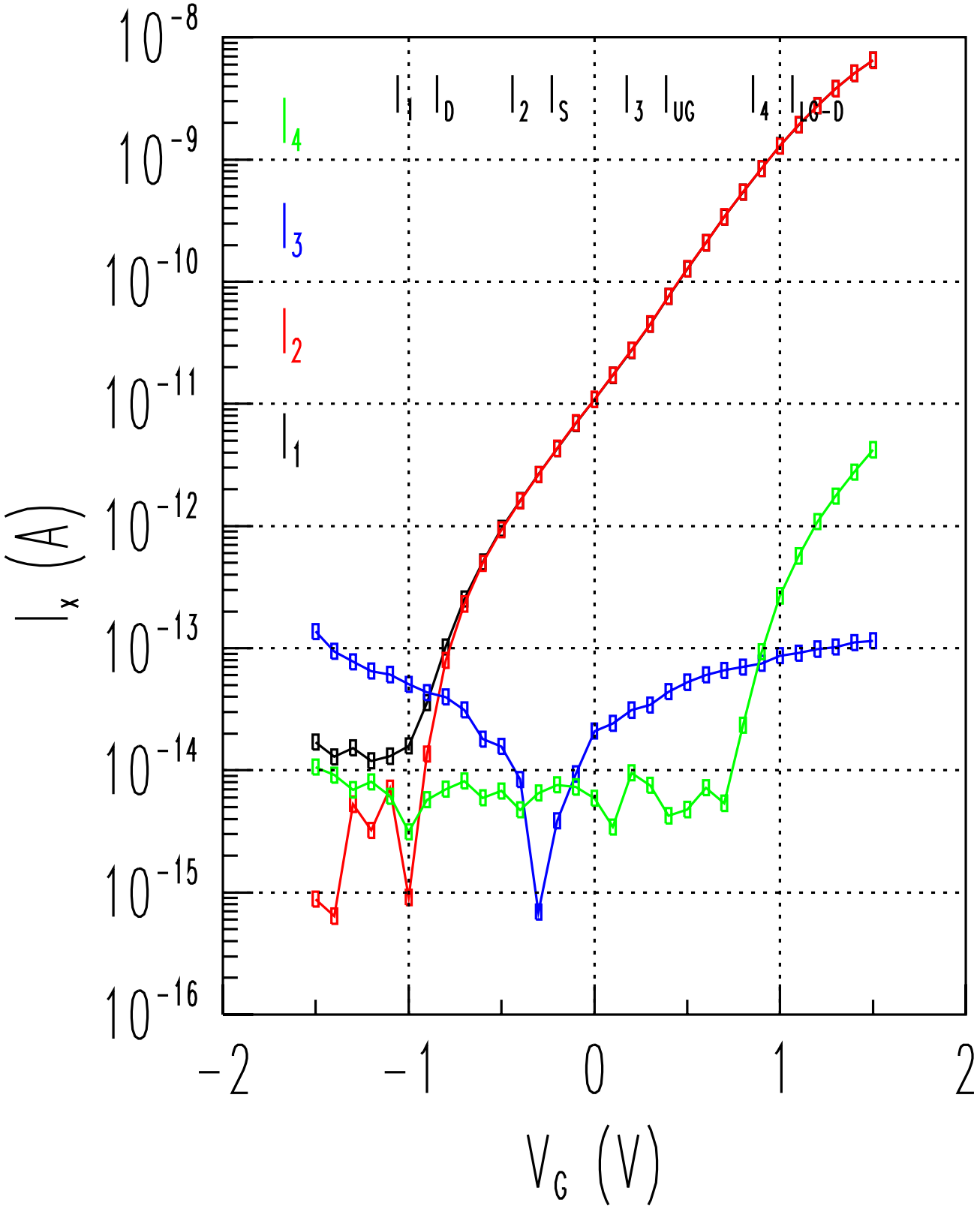
Die 16 3G40

Die 16 SD2 top



Die 16 SD2 bottom

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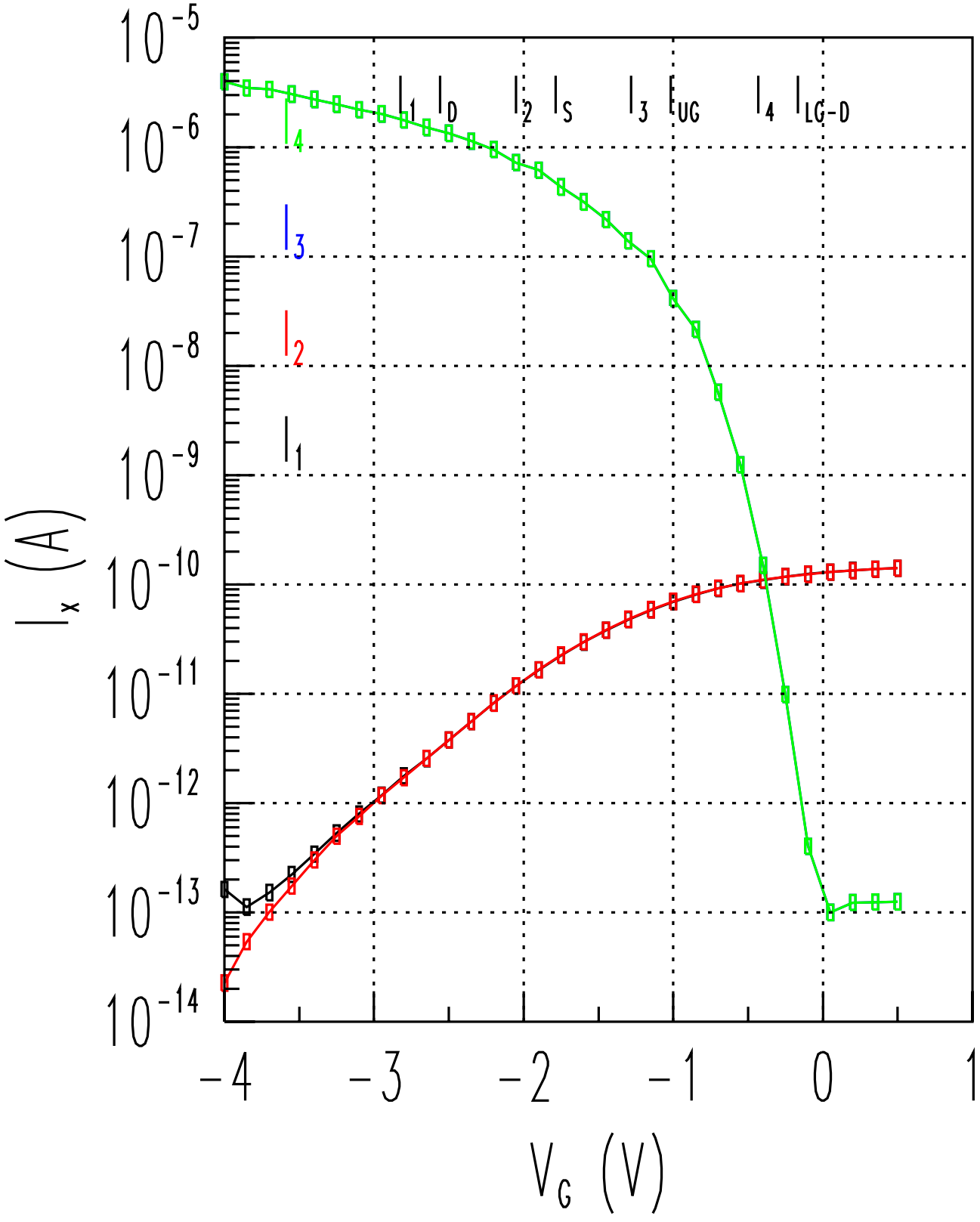
I1 ID I2 IS I3 IUG I4 IG-D
I4
I3
I2
I1
10-8
10-9
10-10
10-11
10-12
10-13
10-14
10-15
10-16
Ix (A)
-2
-1
0
1
2
VG (V)

[-1.5, +1.5] means a scan over that range; sh means the pin is shorted.
In most measurements, all other pins (18 total) are shorted.

filename	D	S	UG	LG-D	LG-C	LG-S	BG	
Aug3_10	"+ 10 mV	0	[-1.5, +1.5]	0	sh	sh	sh	
Aug3_20	"+ 10 mV	0	"+ 0.5 V	[-4.0, +0.5]	sh	sh	sh	
Aug3_21	"+ 10 mV	0	"+ 0.5 V	sh	[-4.0, +0.5]	sh	sh	
Aug3_22	"+ 10 mV	0	"+ 0.5 V	sh	sh	[-4.0, +0.5]	sh	
Aug4_5	"+ 10 mV	0	[-1.5, + 2.0]	0	sh	sh	sh	
Aug4_13	"+ 10 mV	0	"+ 0.5 V	[-5.0, +0.5]	sh	sh	sh	
Aug19_40	"+ 10 mV	0	sh	"+ 1.0	floating	floating	[-2, +2]	all other pins floating
Aug19_42	"+ 10 mV	0	sh	[-5, +1]	floating	floating	"-1.0	all other pins floating
Aug19_15	0	0	0	floating	floating	floating	[-5, +5]	all other pins floating
Aug22_20	"+10 mV	0	none	0	floating	floating	[-1, +2]	pins 1-8 unshorted
Aug22_18	"+10 mV	0	none	0	floating	floating	[-1, +2]	pins 1-9 unshorted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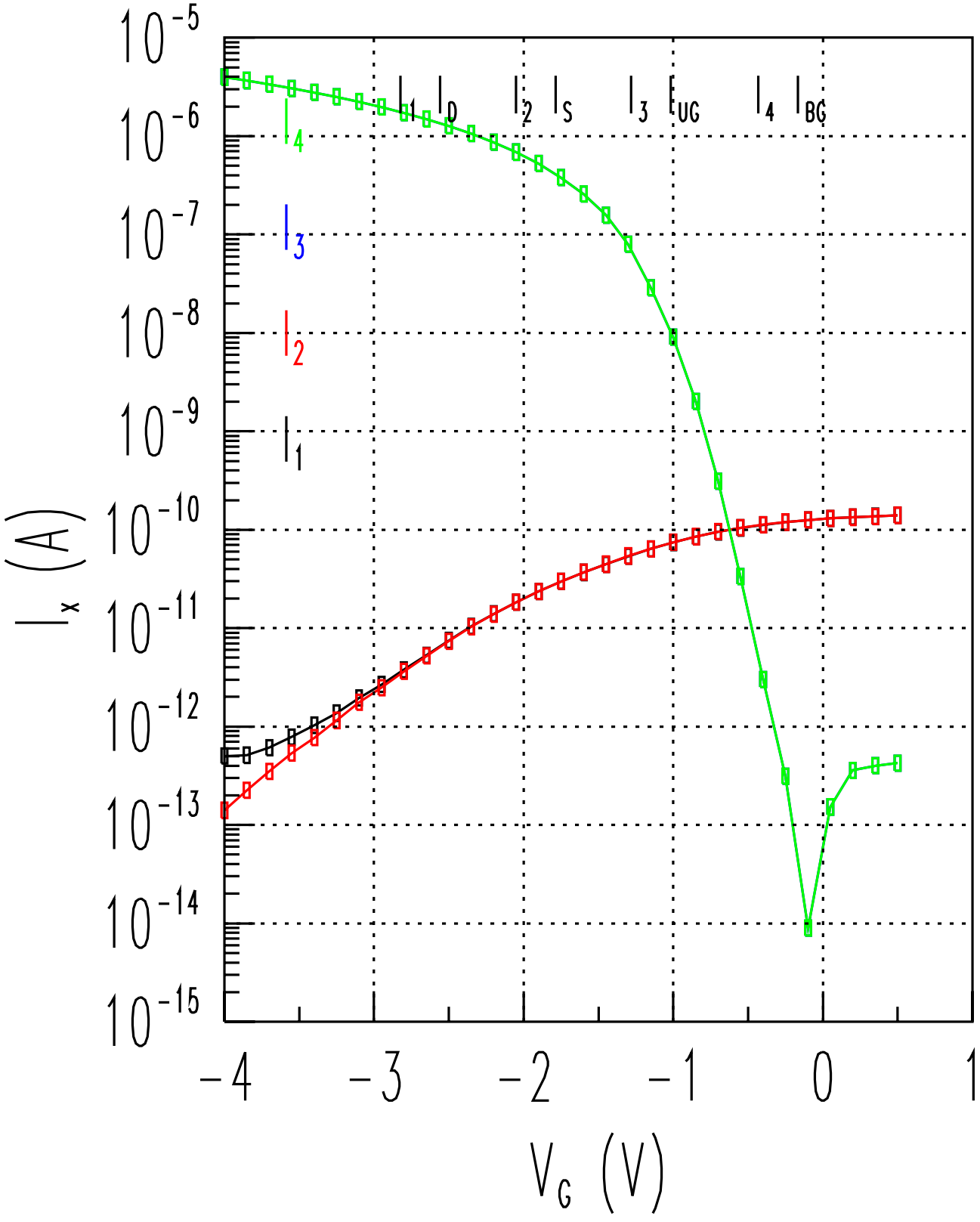
I1 ID I2 IS I3 IUG I4 ILG-D
4
3
2
1
10-5
10-6
10-7
10-8
10-9
10-10
10-11
10-12
10-13
10-14
Ix (A)
-4
-3
-2
-1
0
1
VG (V)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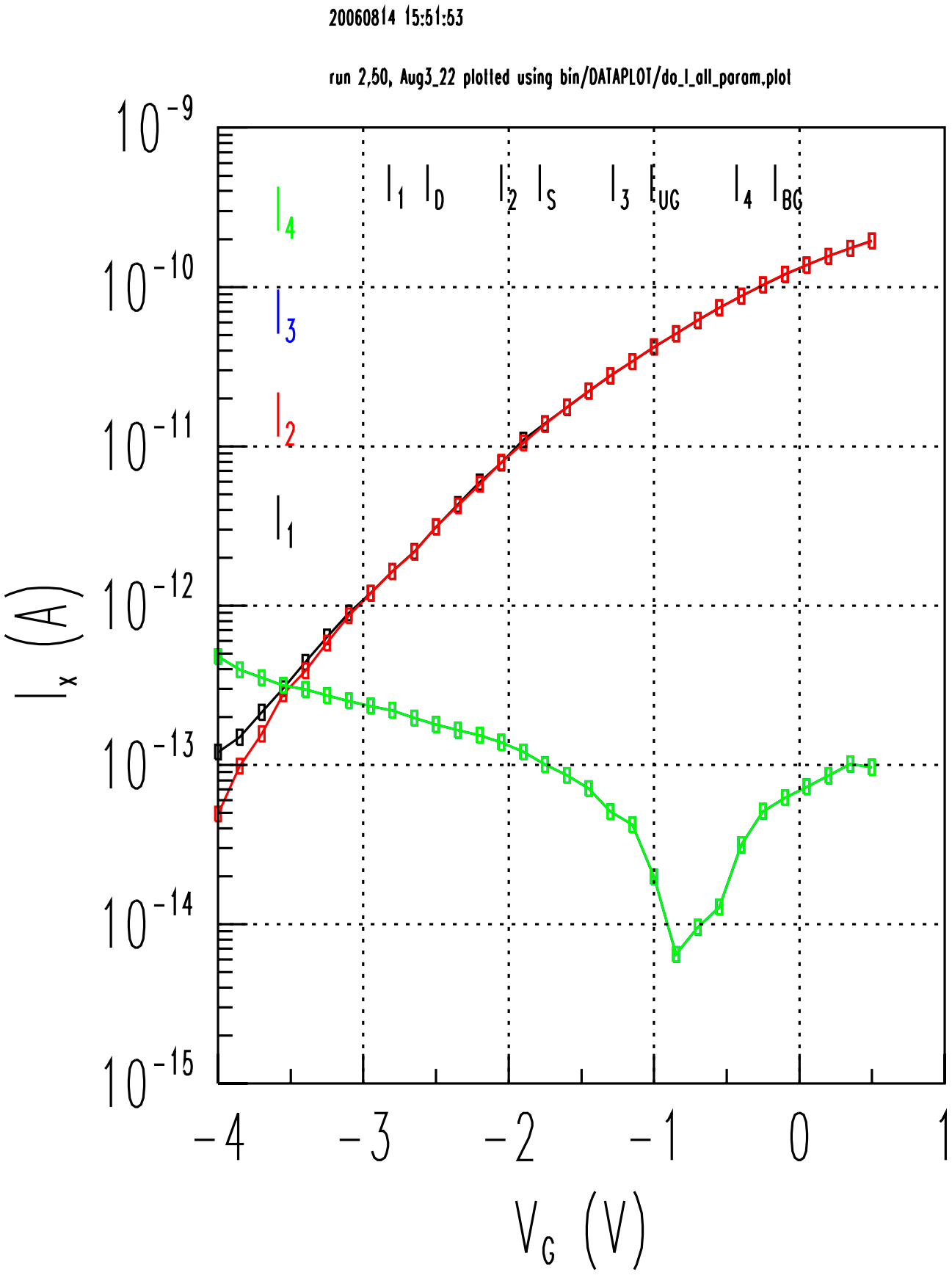
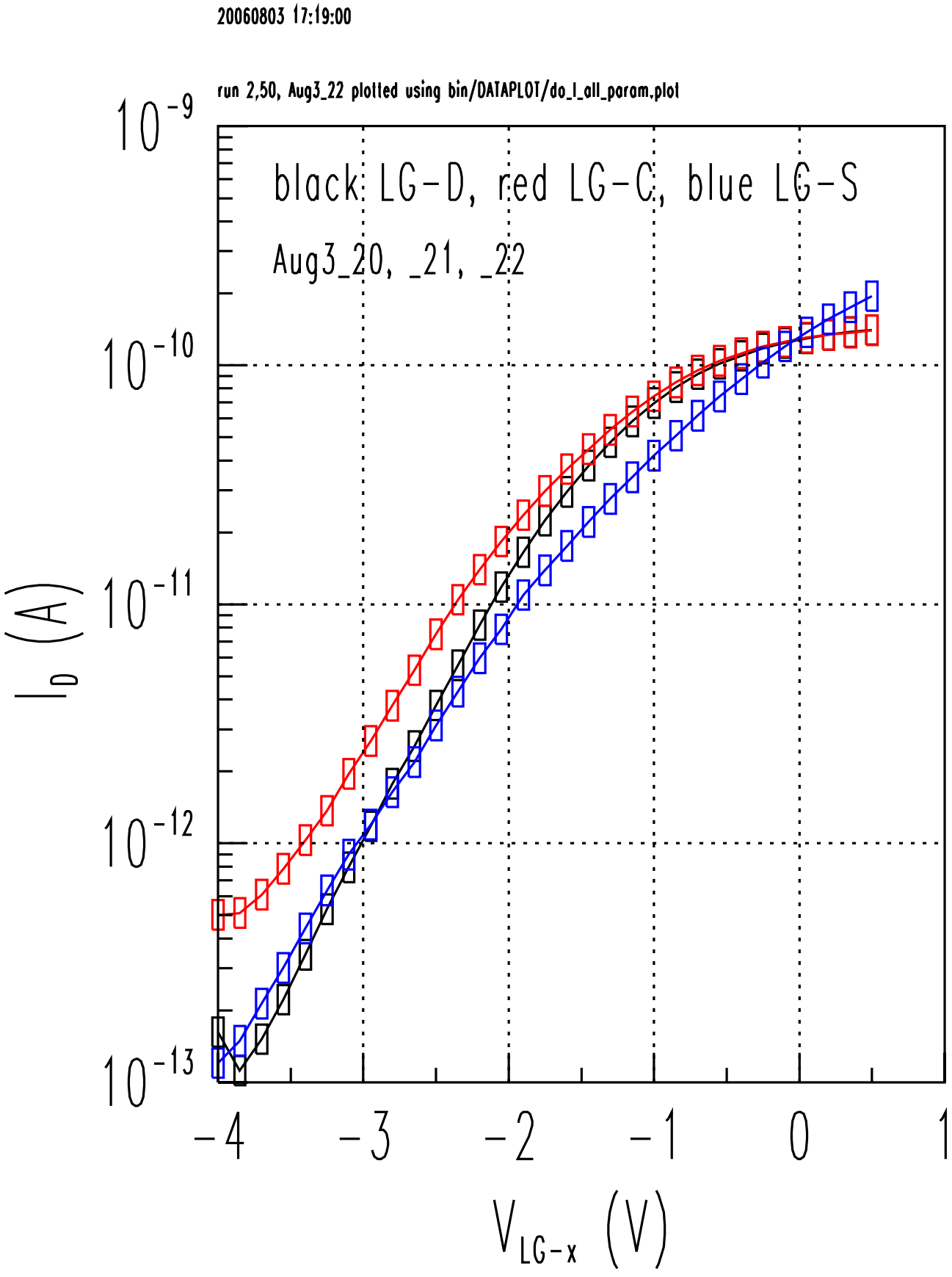
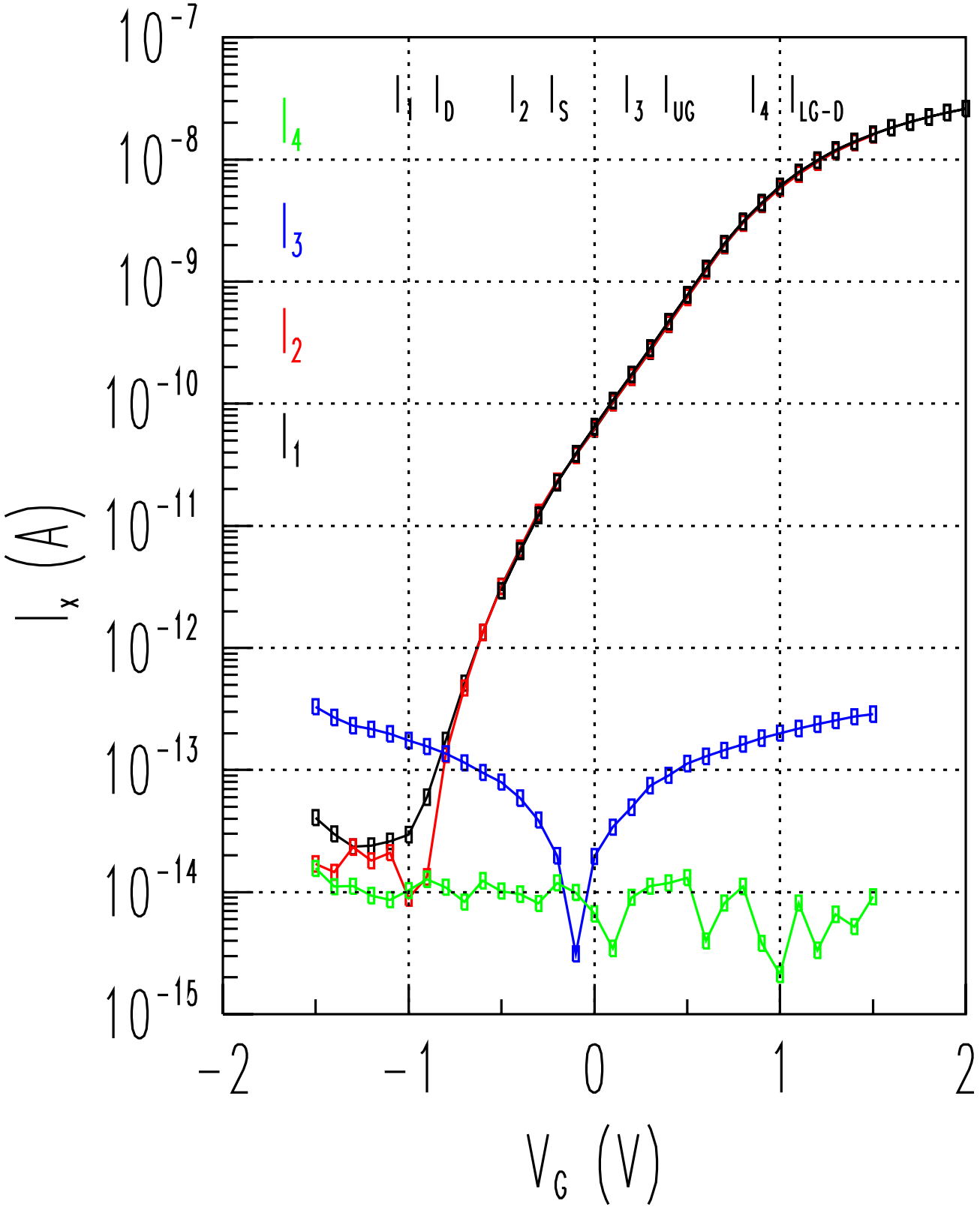
run 2,50, Aug3_21 plotted using bin/DATAPLOT/do_I_all_param.plot
I1 ID I2 IS I3 IUG I4 IBG
4
3
2
1
10-5
10-6
10-7
10-8
10-9
10-10
10-11
10-12
10-13
10-14
10-15
Ix (A)
-4
-3
-2
-1
0
1
VG (V)


20060814 15:51:53
run 2,50, Aug3_22 plotted using bin/DATAPLOT/do_I_all_param.plot
I1 ID I2 IS I3 IUG I4 IBG
I4
I3
I2
I1
10-9
10-10
10-11
10-12
10-13
10-14
10-15
Ix (A)
-4
-3
-2
-1
0
1
VG (V)


20060803 17:19:00
run 2,50, Aug3_22 plotted using bin/DATAPLOT/do_I_all_param.plot
black LG-D, red LG-C, blue LG-S
Aug3_20, _21, _22
10^-9
10^-10
10^-11
10^-12
10^-13
I_D (A)
-4
-3
-2
-1
0
1
V_LG-x (V)


20060804 14:43:10
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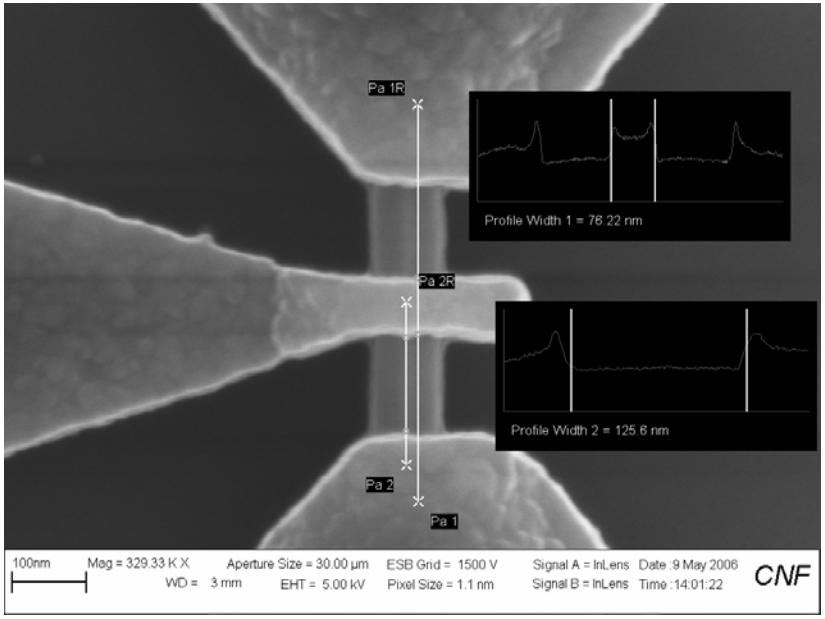
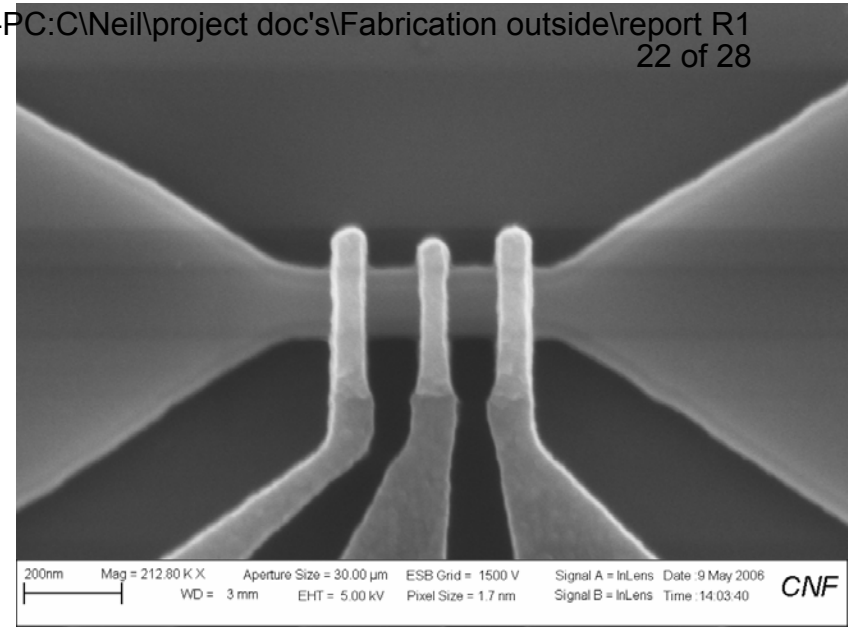
I1 ID I2 IS I3 IUG I4 ILG-D
I4
I3
I2
I1
10-7
10-8
10-9
10-10
10-11
10-12
10-13
10-14
10-15
Ix (A)
-2
-1
0
1
2
VG (V)

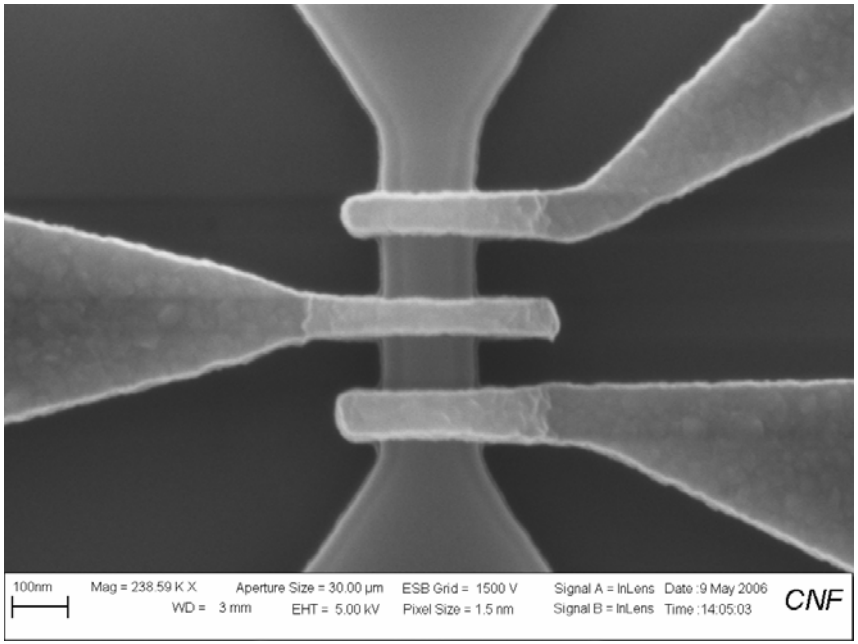


Die 17 HT40

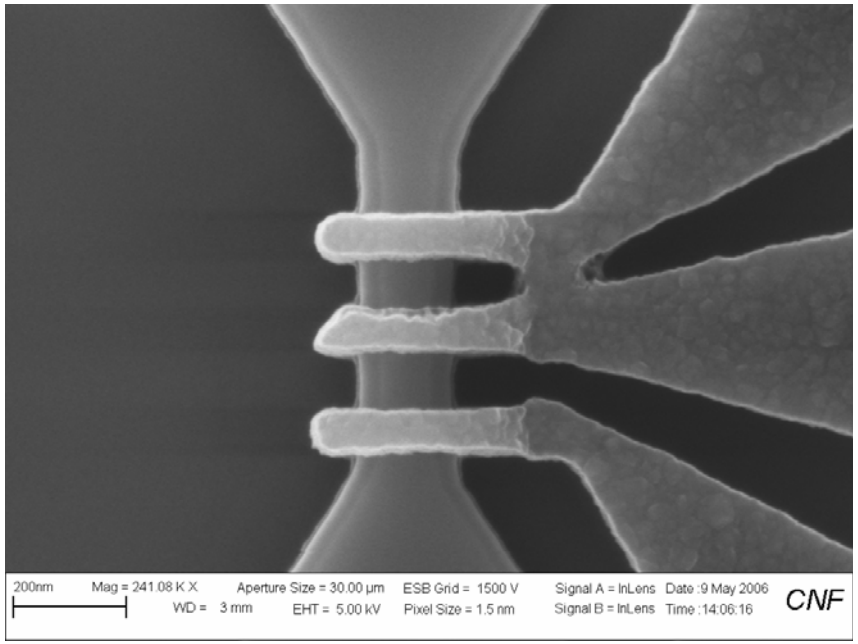


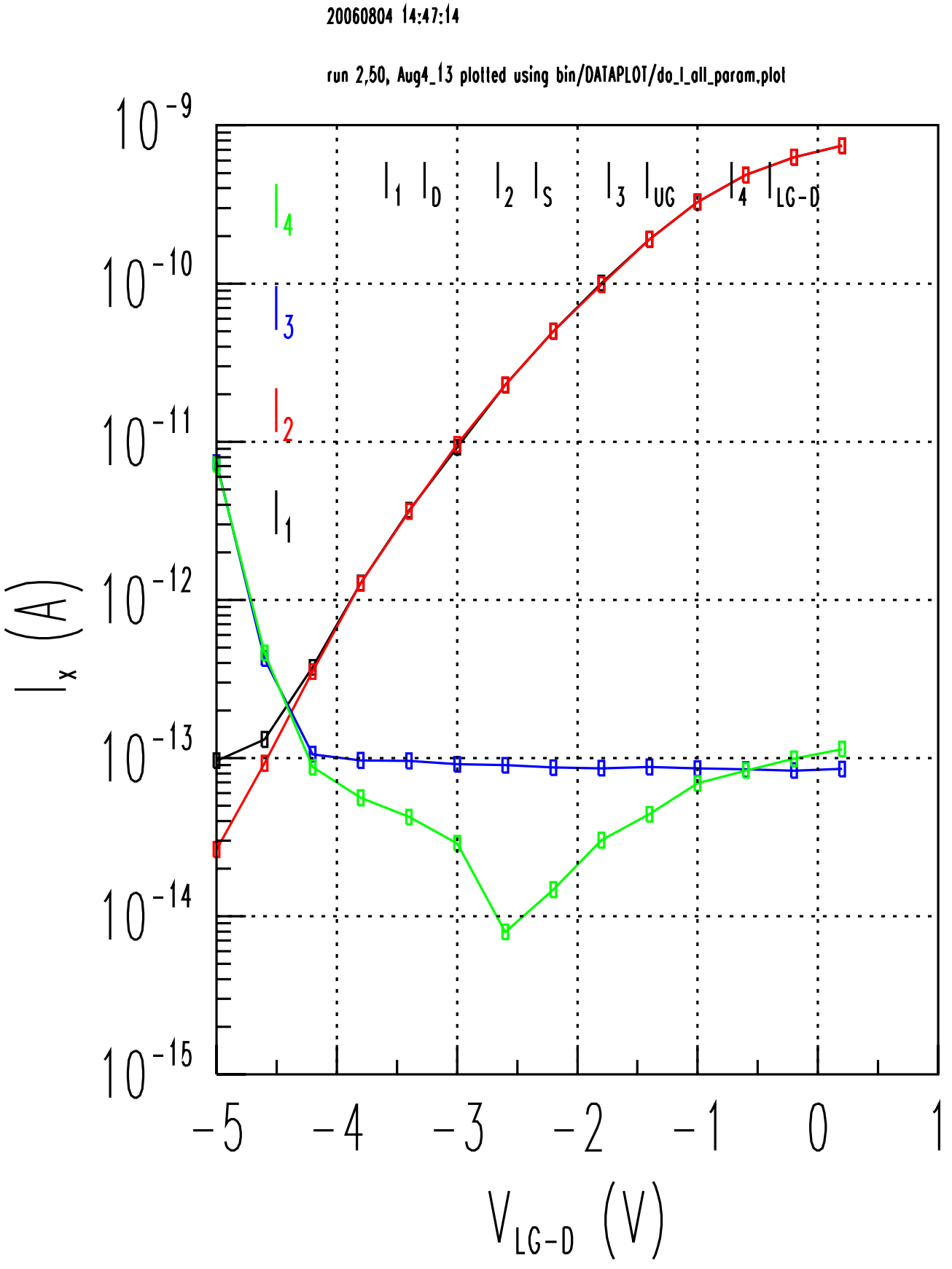
Die 17 3G40

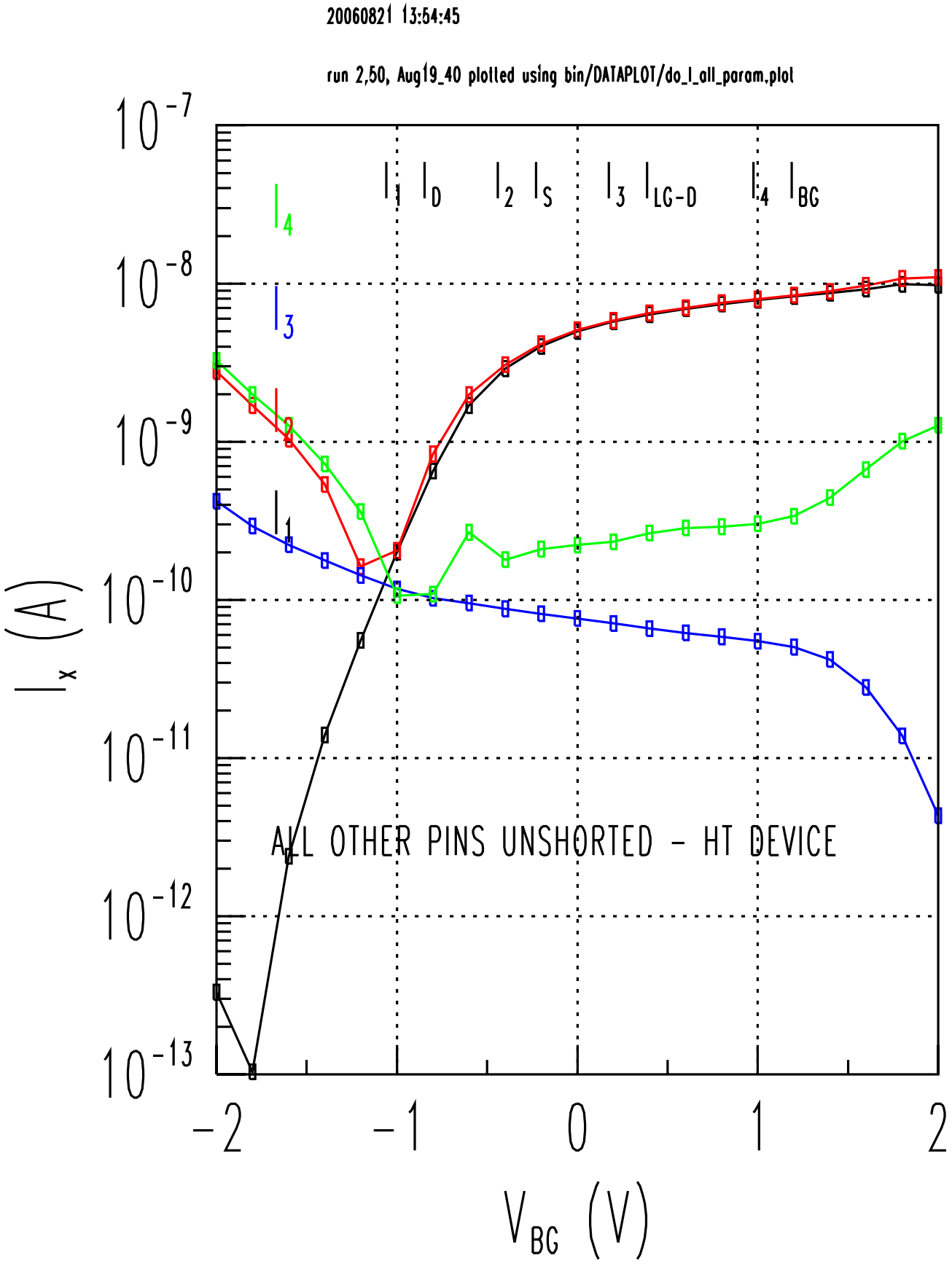
Die 17 SD2 top

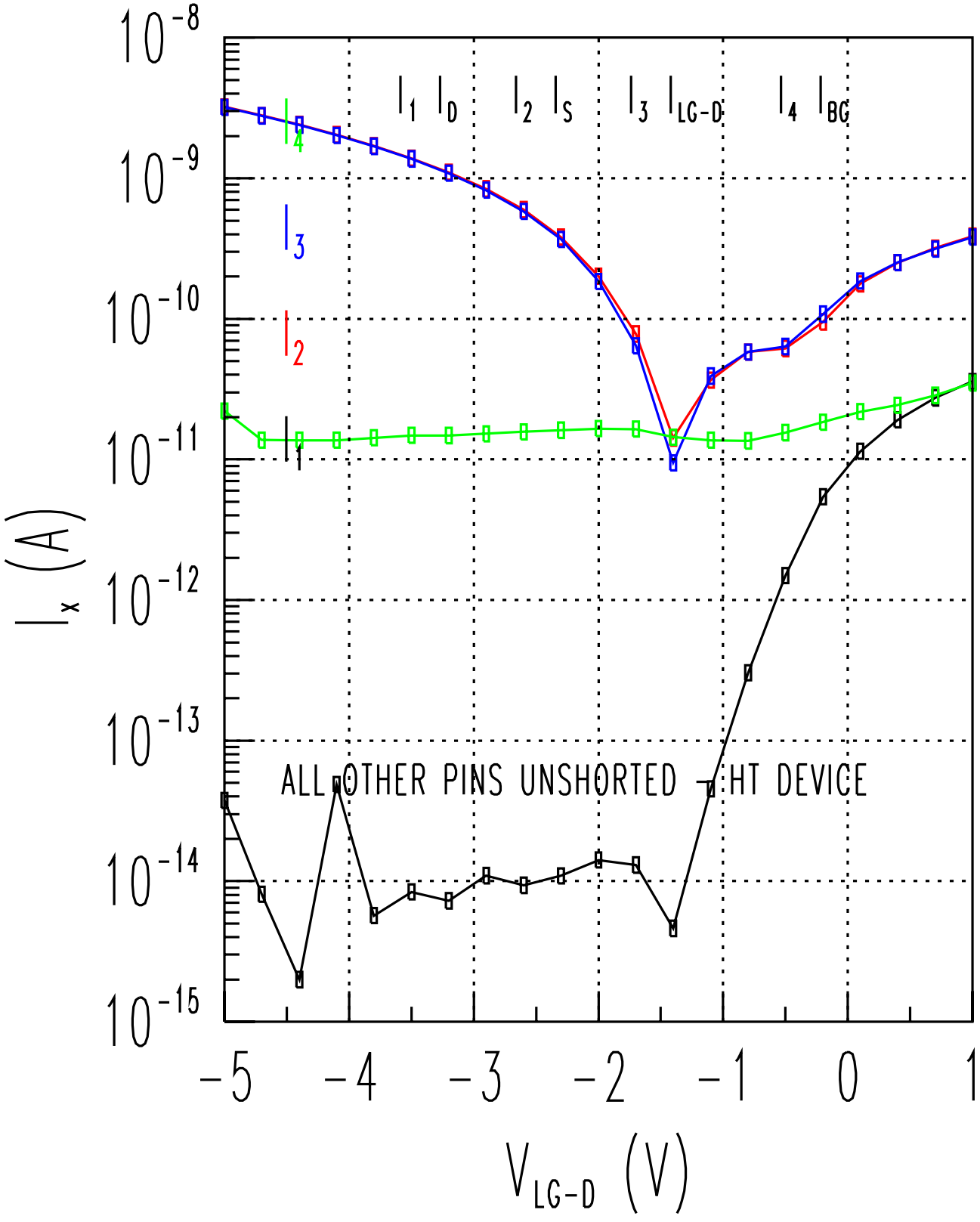


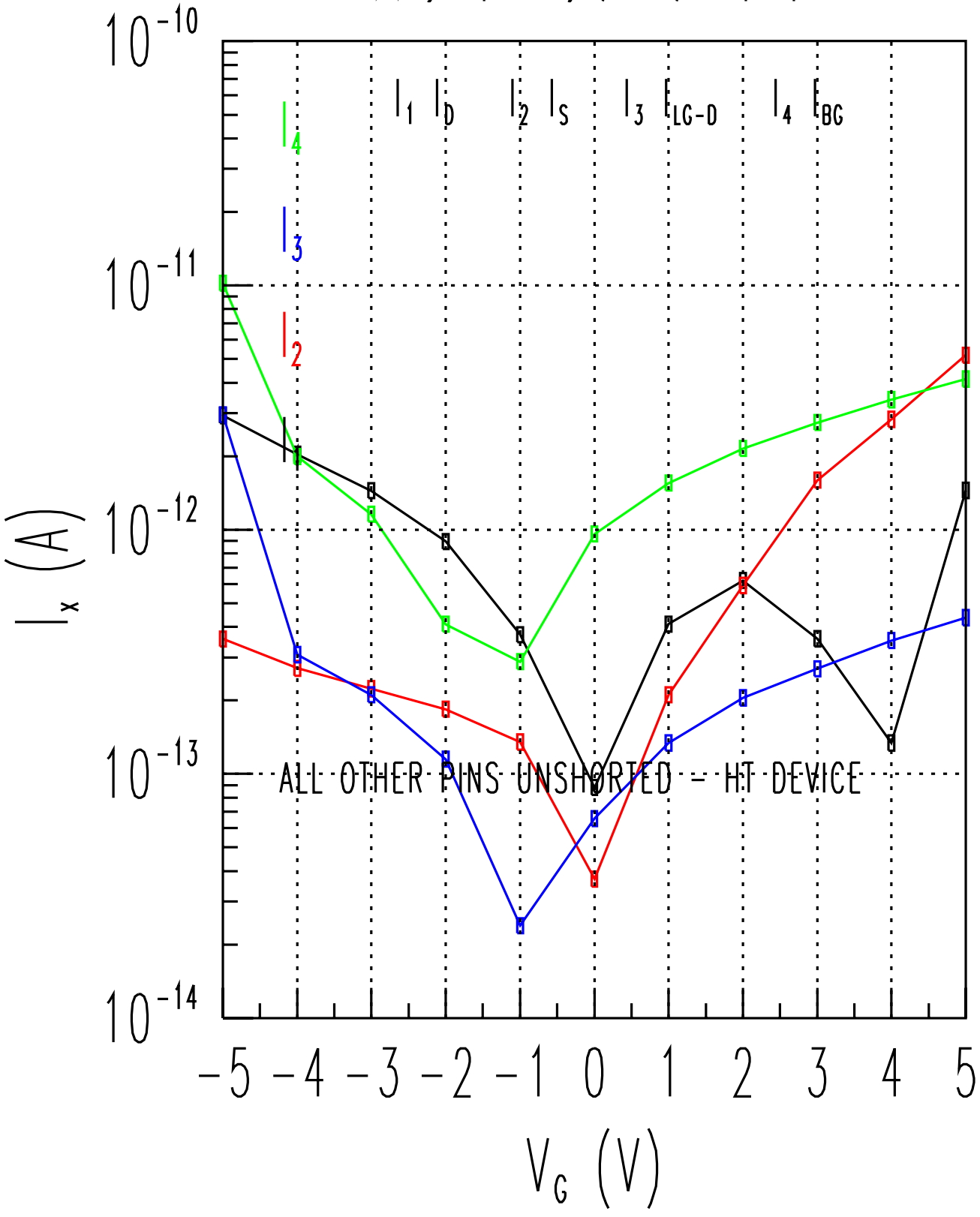
Die 17 SD2 bottom

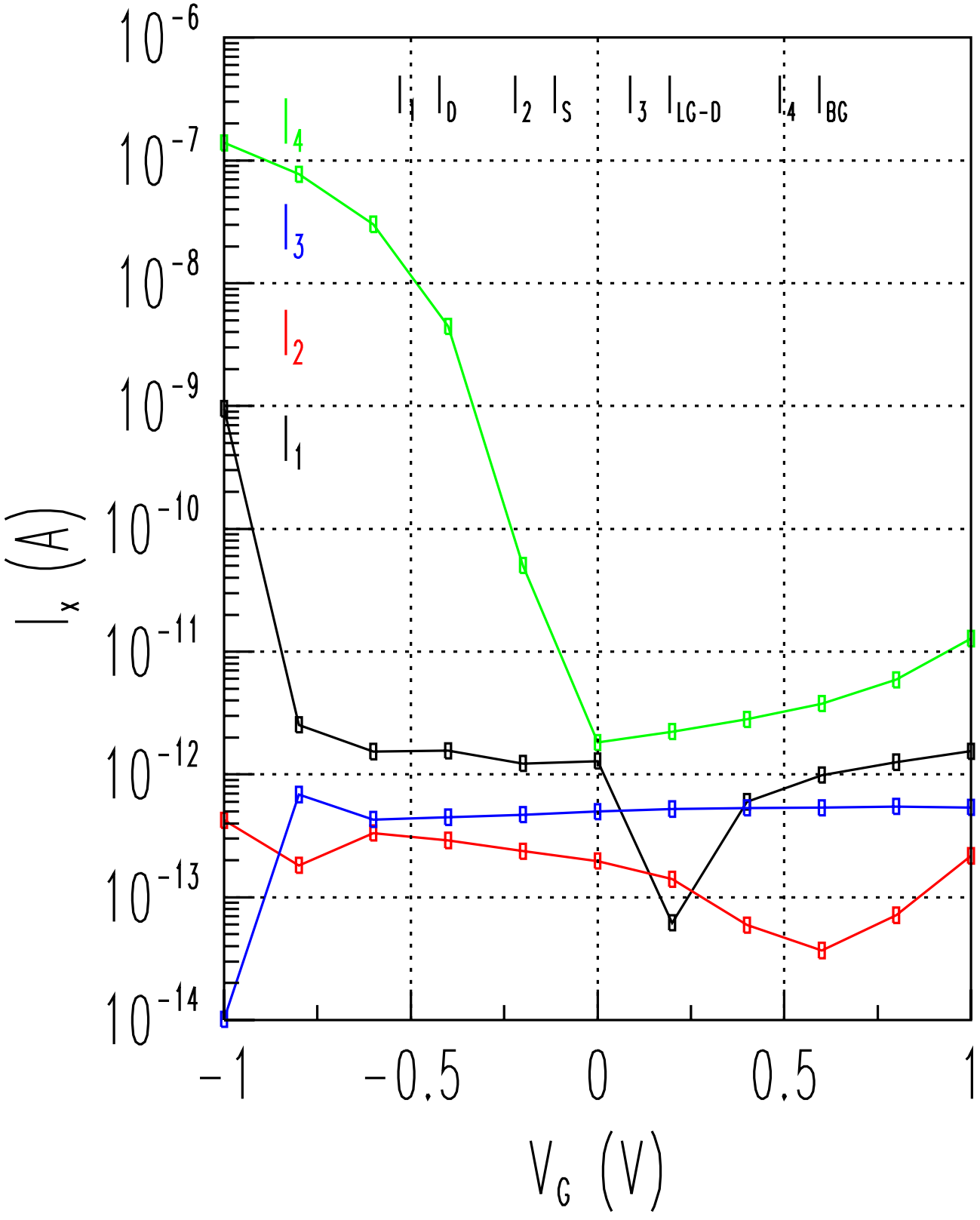


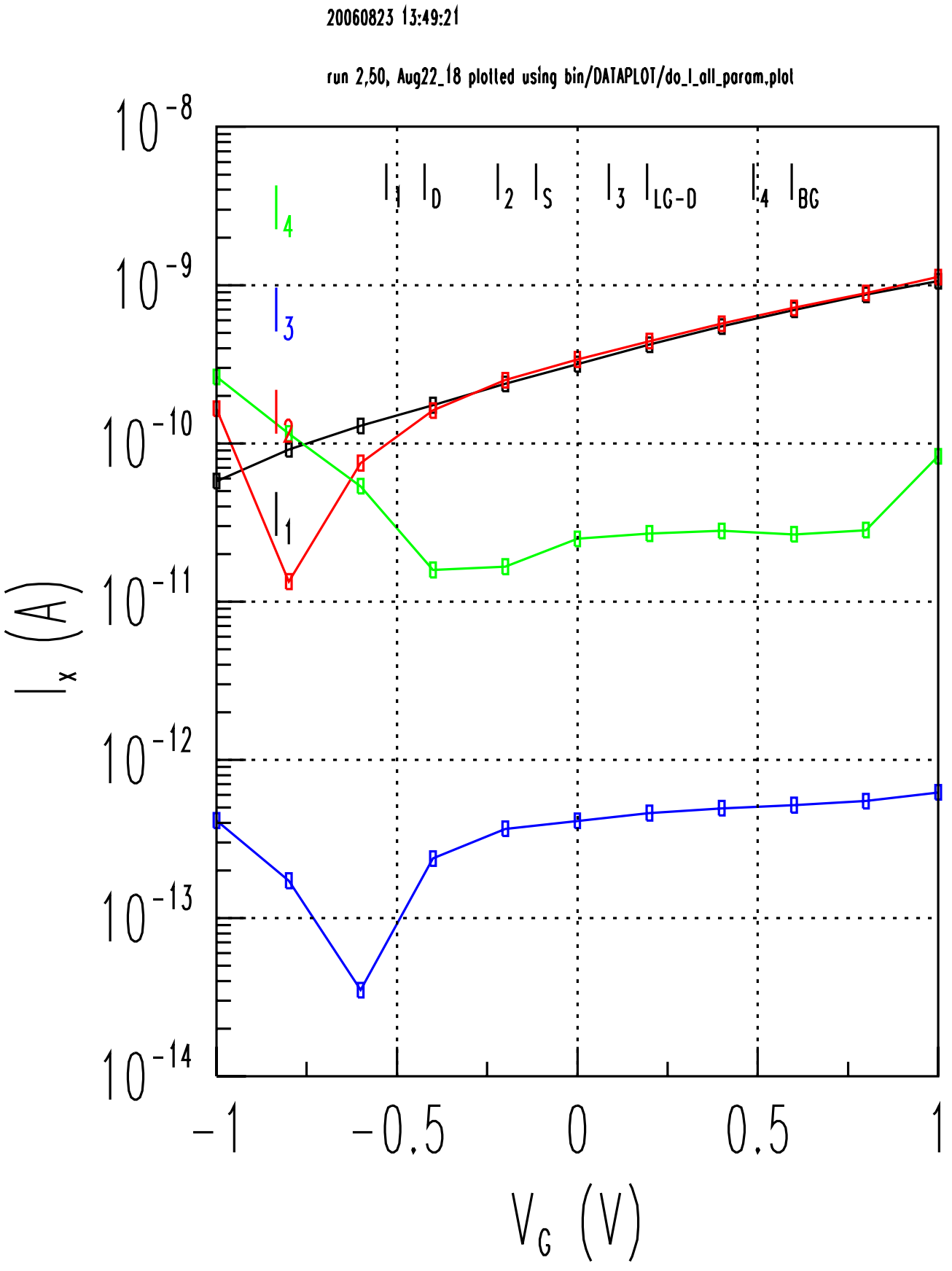

20060804 14:47:14
run 2,50, Aug4_13 plotted using bin/DATAPLOT/do_I_all_param.plot
I1 ID I2 IS I3 IUG I4 ILG-D
I4
I3
I2
I1
Ix (A)
10-9
10-10
10-11
10-12
10-13
10-14
10-15
-5 -4 -3 -2 -1 0 1
VLG-D (V)


20060821 13:54:45
run 2,50, Aug19_40 plotted using bin/DATAPLOT/do_I_all_param.plot
I1 ID I2 IS I3 ILG-D I4 IBG
I4
I3
I1
ALL OTHER PINS UNSHORTED - HT DEVICE
Ix (A)
VBG (V)
10-7
10-8
10-9
10-10
10-11
10-12
10-13
-2
-1
0
1
2


20060821 13:57:25
run 2,50, Aug19_42 plotted using bin/DATAPLOT/do_I_all_param.plot
I1 ID
I2 IS
I3 ILG-D
I4 IBG
4
3
2
1
ALL OTHER PINS UNSHORTED - HT DEVICE
10-8
10-9
10-10
10-11
10-12
10-13
10-14
10-15
Ix (A)
-5
-4
-3
-2
-1
0
1
VLG-D (V)


20060822 10:42:08
run 2,50, Aug19_15 plotted using bin/DATAPLOT/do_I_all_param.plot
I1 ID I2 IS I3 ILG-D I4 IBG
4
3
2
ALL OTHER PINS UNSHORTED - HT DEVICE
10-10
10-11
10-12
10-13
10-14
Ix (A)
-5 -4 -3 -2 -1 0 1 2 3 4 5
VG (V)


20060823 13:48:49
run 2,50, Aug22_20 plotted using bin/DATAPLOT/do_I_all_param.plot
I1 ID I2 IS I3 ILG-D I4 IBG
I4
I3
I2
I1
10-6
10-7
10-8
10-9
10-10
10-11
10-12
10-13
10-14
Ix (A)
-1
-0.5
0
0.5
1
VG (V)


20060823 13:49:21
run 2,50, Aug22_18 plotted using bin/DATAPLOT/do_I_all_param.plot
I1 ID I2 IS I3 ILG-D I4 IBG
I4
I3
I2
I1
10-8
10-9
10-10
10-11
10-12
10-13
10-14
Ix (A)
-1
-0.5
0
0.5
1
VG (V)

5 Cross-sectional Results

5.1 fine area of 3G device

Please see the micrographs in the next five pages. On the left side is a purple line indicating where the cross-sectional cut is made (this graph is without the upper gate). We can see the following:

BOX swells slightly near edge of SOI

LG
1. fingers look well-formed when not on top of SOI wire
2. near or on top of wire, they get narrower and much thicker - this is not understood.

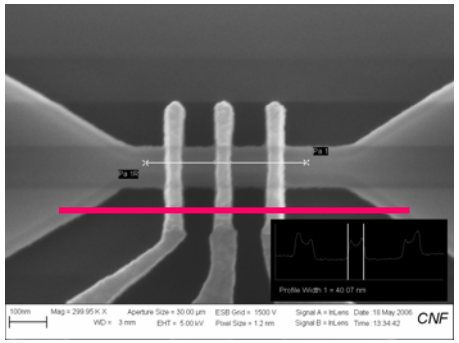
UG this looks good, fills in well around and between LG's.

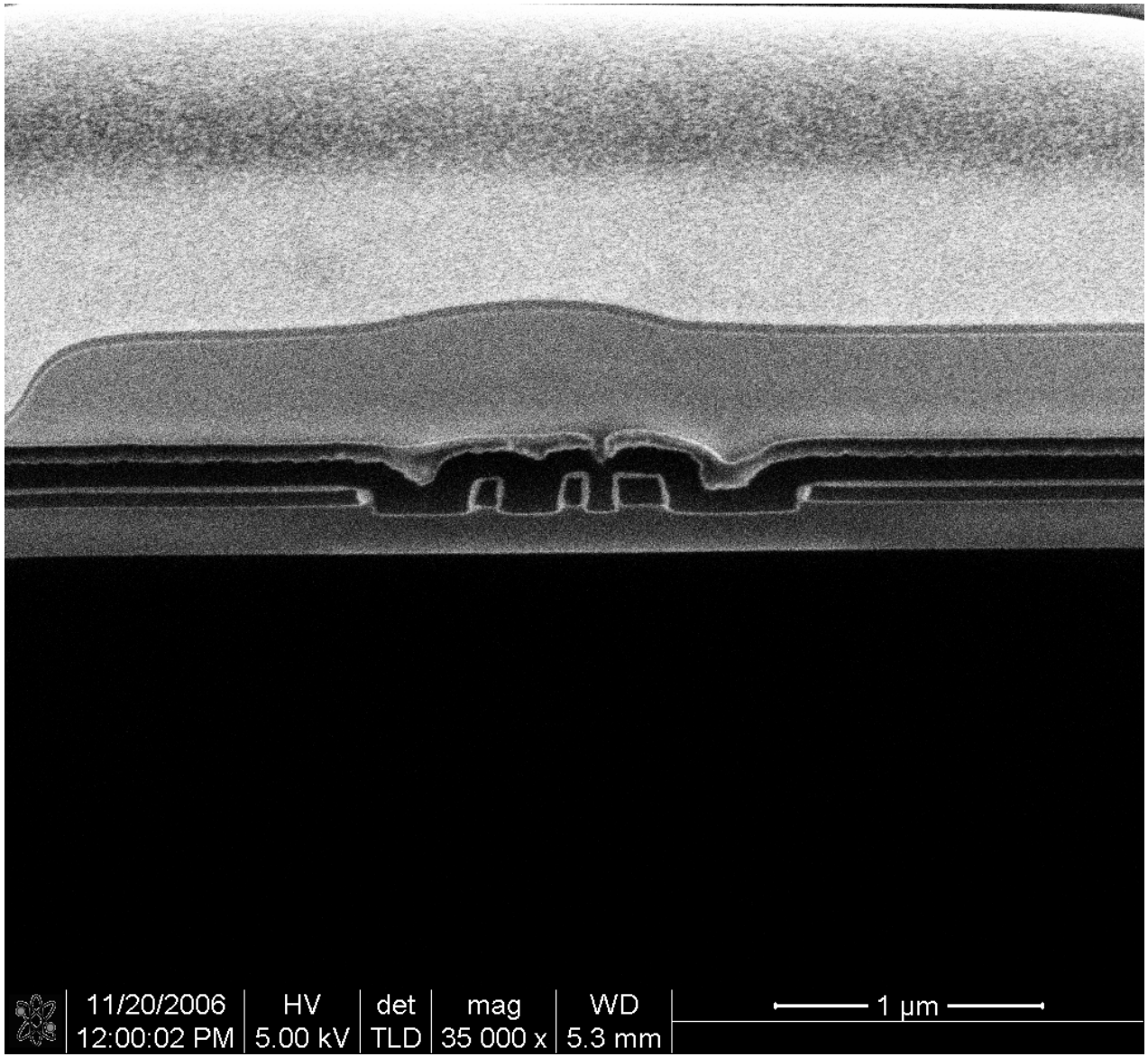
In the three micrographs after this, we can see the overlap regions. These are regions where we have etched away the oxide on top of the UG, LG and SOI in order to make contact to the deposited metal.

The etching step is 90 seconds of 6:1 buffered oxide etch (BOE). Clearly, this step is way too aggressive, because it has etched away the BOX completely in some places, and partially in others. We will not perform this same etching step in the future.

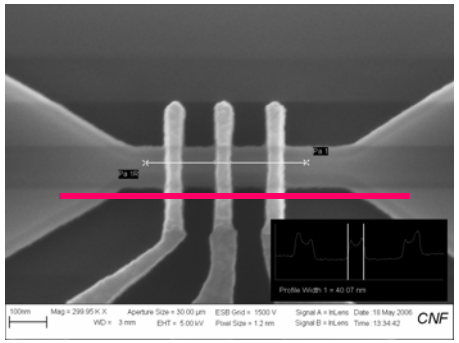
We also note that the LG is either pitted or etched away completely in these areas, which may be a result of the UG etch, if the thermal oxide on the LG did not form a good protective layer. Note for the future: the new, CMOS-dedicated CL_2 etcher will never have F-based etching gasses in it; this may alleviate the problem of attacking the LG during the UG etching step.

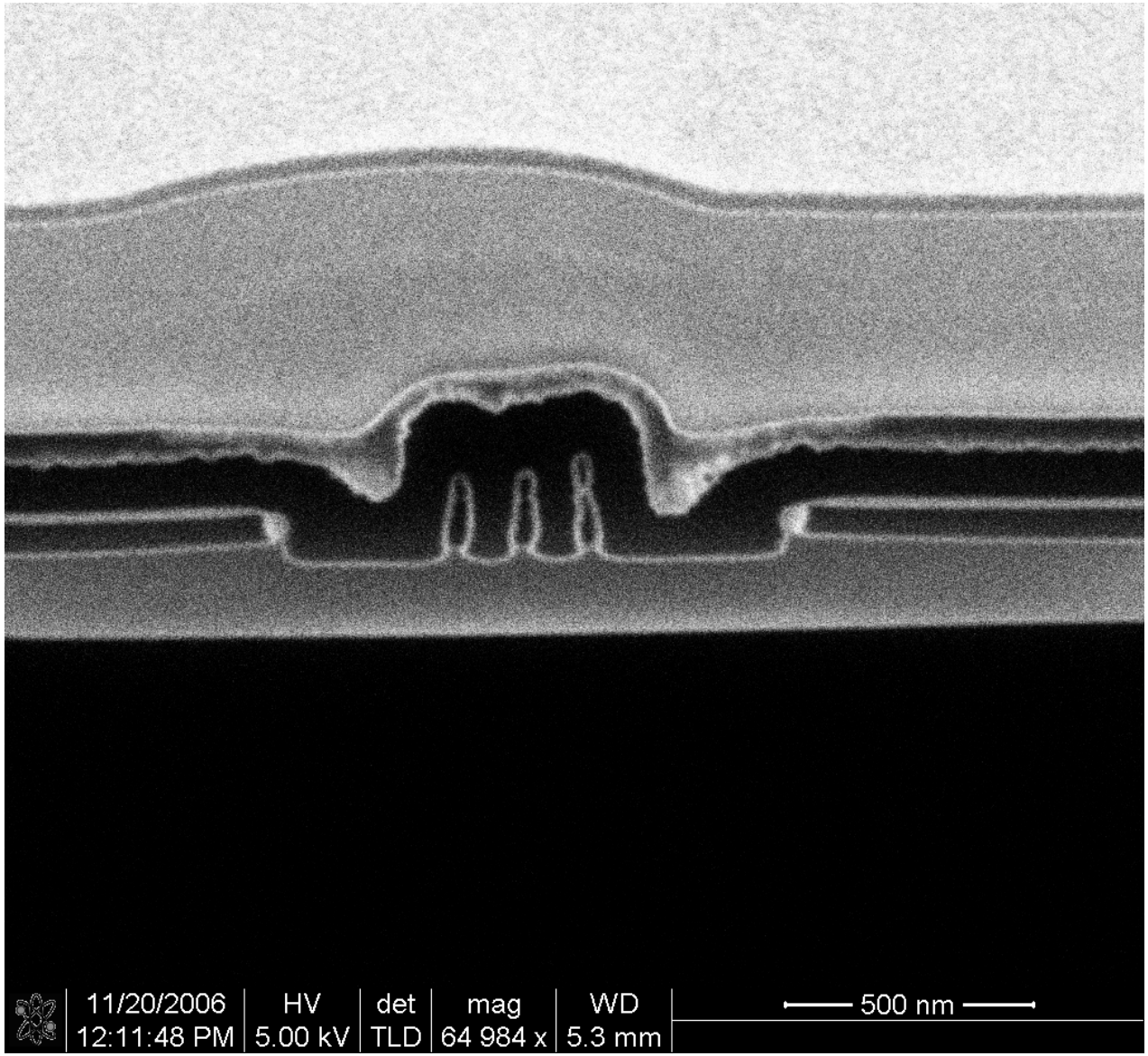
JW 1.7 Die 8 3G



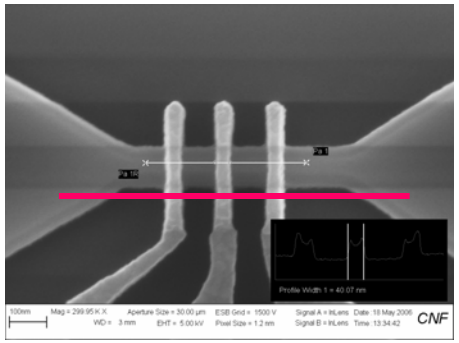


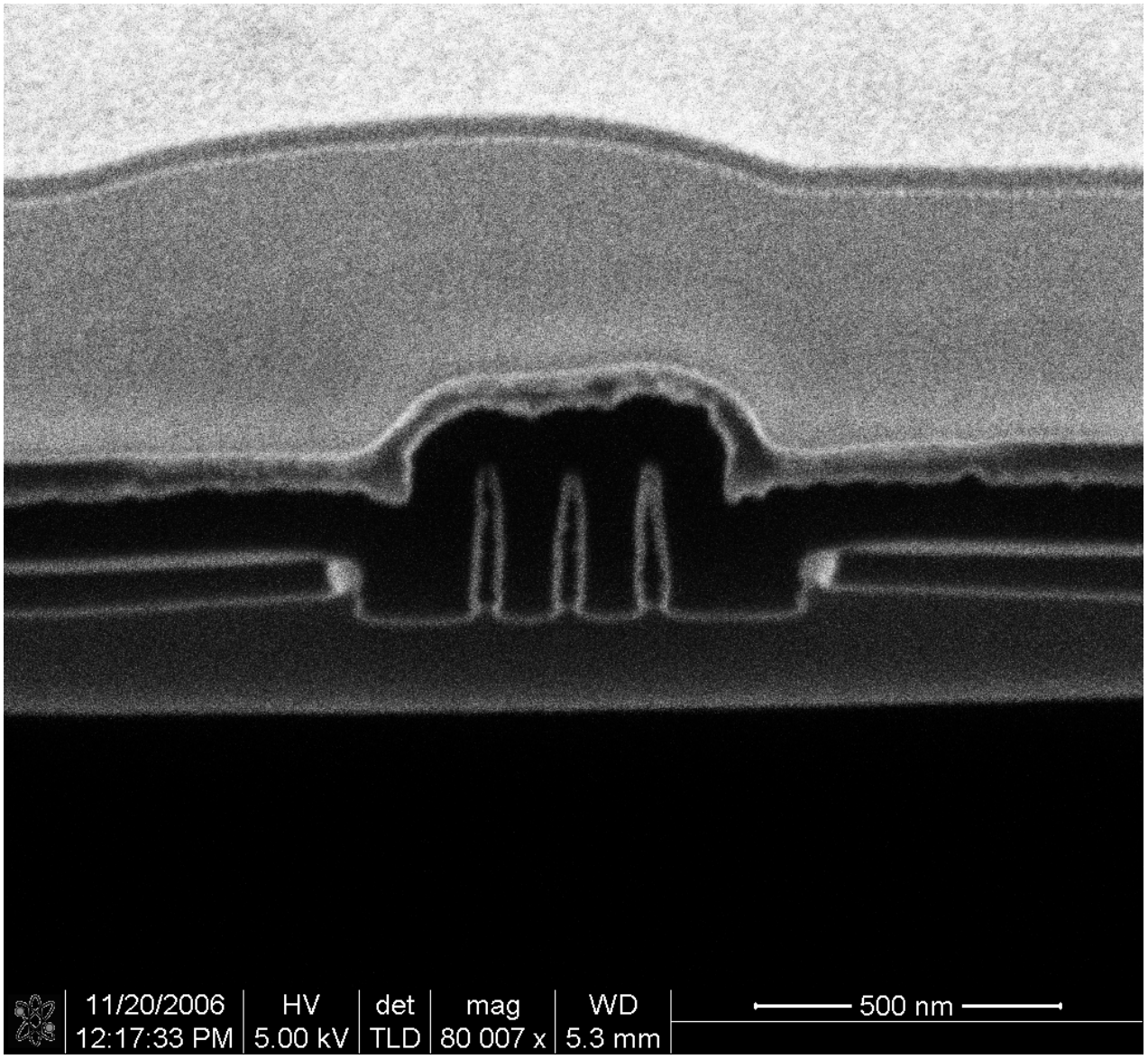
JW 1.7 Die 8 3G



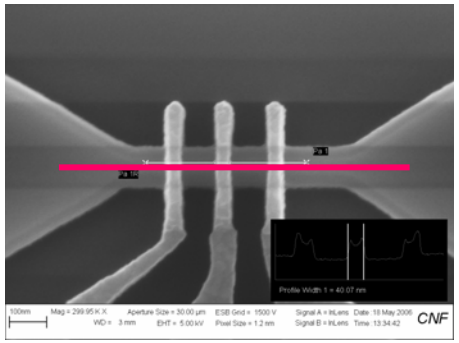


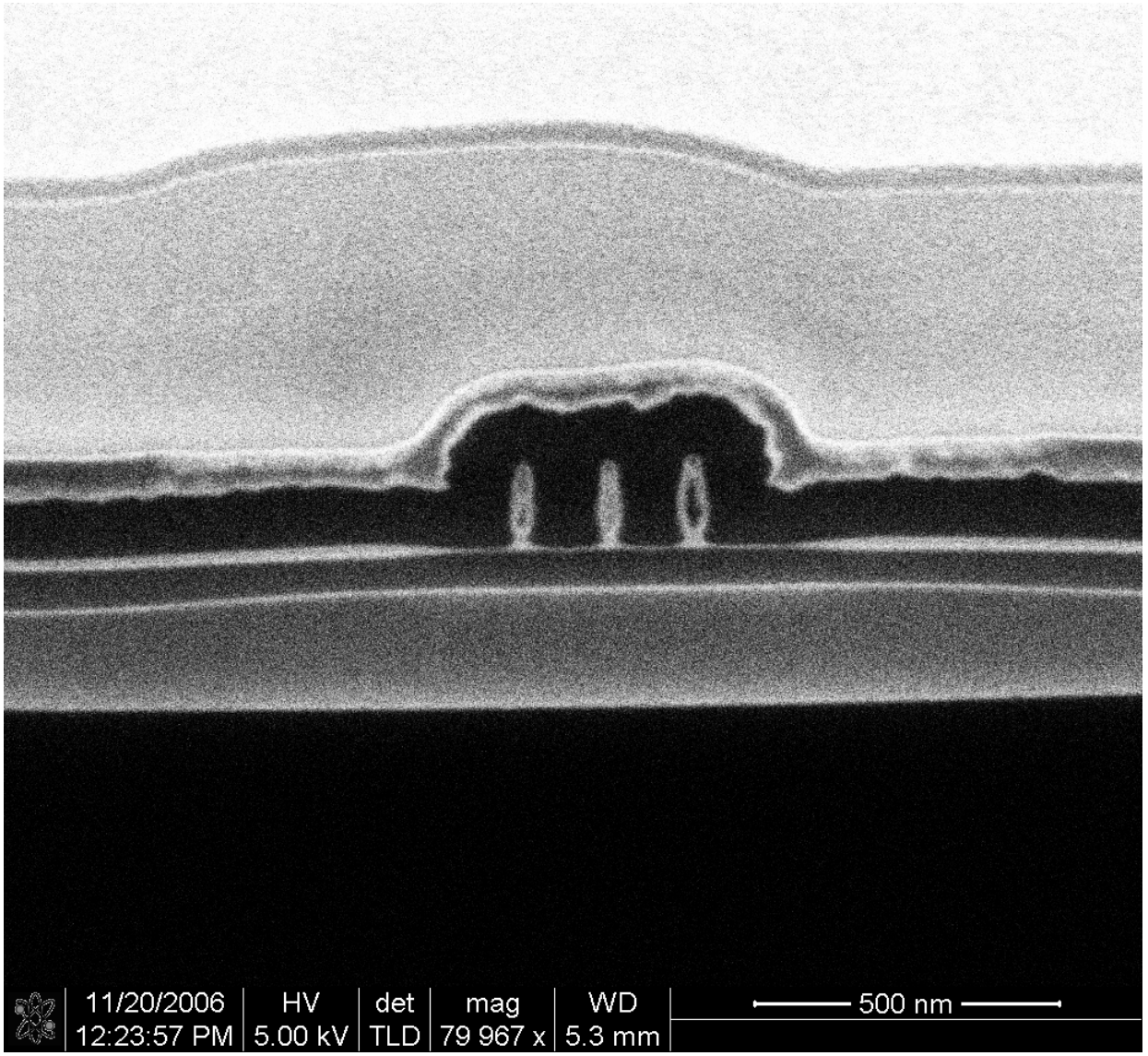
JW 1.7 Die 8 3G


Profile Width 1 = 40.07 nm
CNF

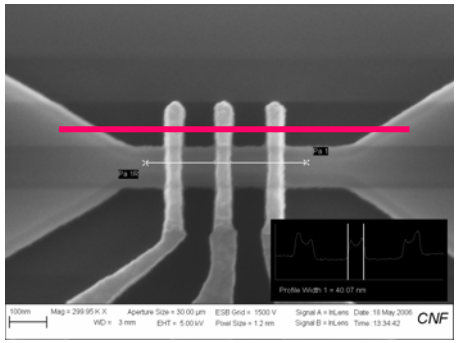

11/20/2006
12:17:33 PM
HV
5.00 kV
det
TLD
mag
80 007 x
WD
5.3 mm
500 nm

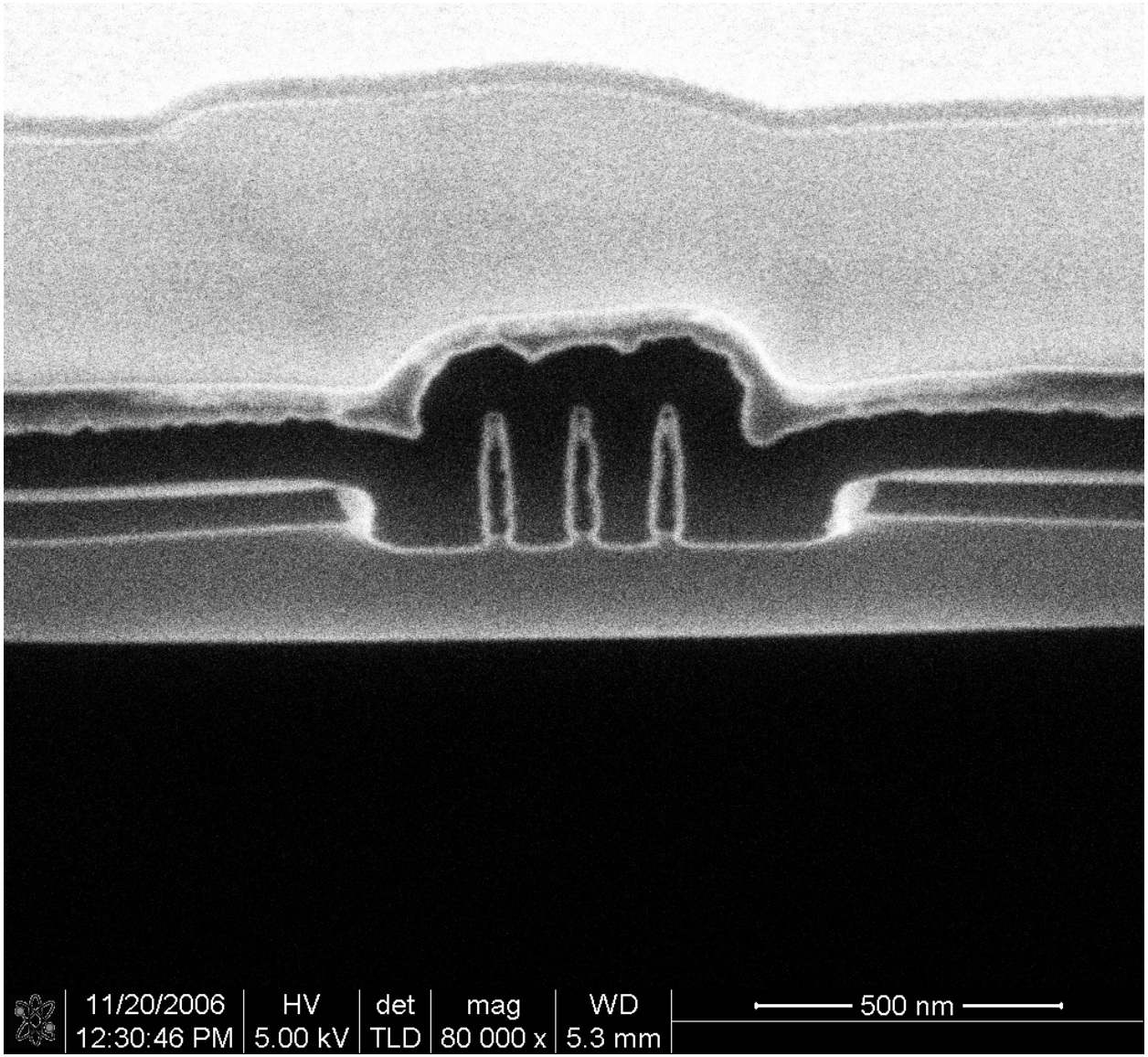
JW 1.7 Die 8 3G


CNF

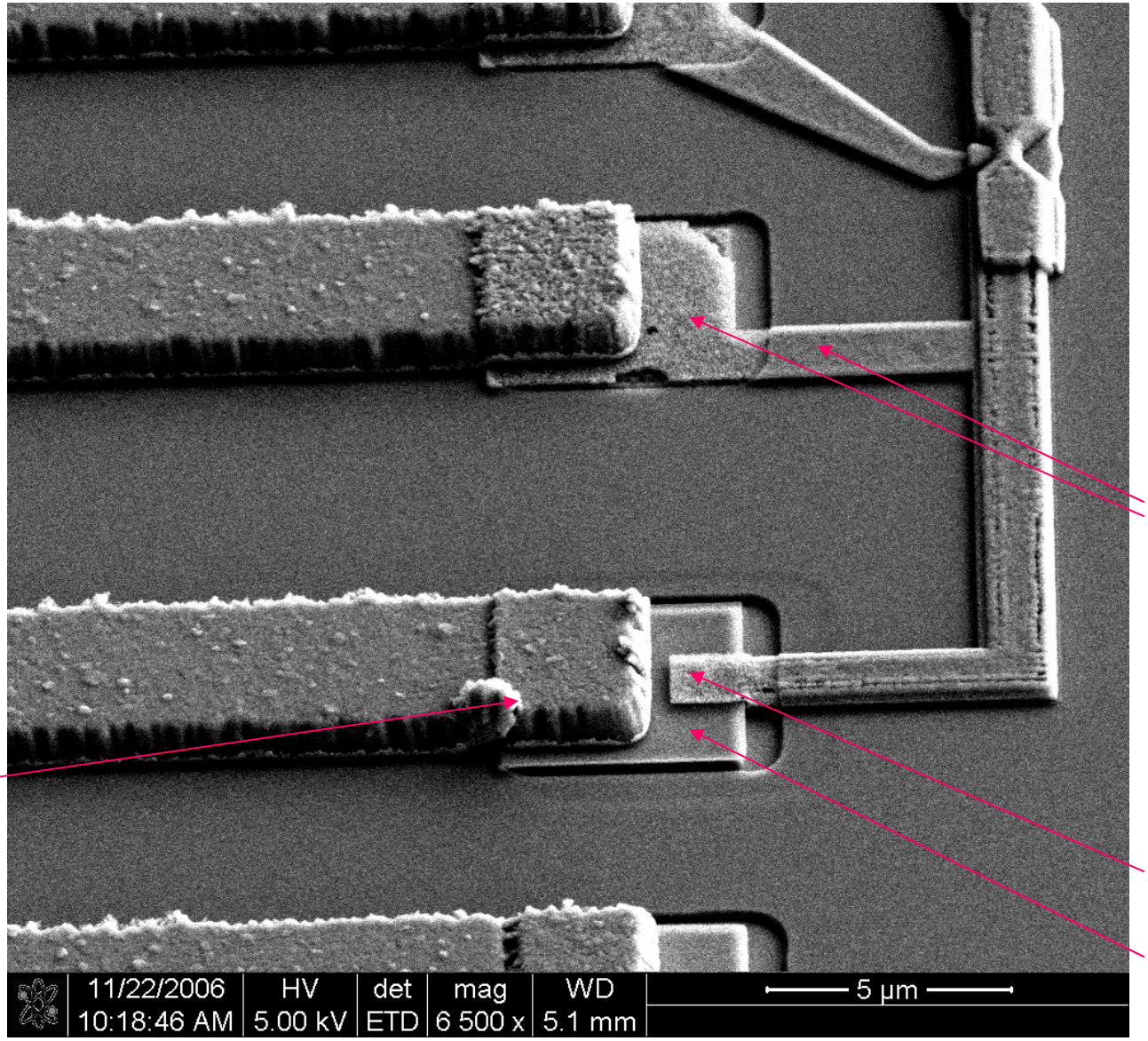

11/20/2006
12:23:57 PM
HV
5.00 kV
det
TLD
mag
79 967 x
WD
5.3 mm
500 nm

JW 1.7 Die 8 3G


CNF


11/20/2006
12:30:46 PM
HV
5.00 kV
det
TLD
mag
80 000 x
WD
5.3 mm
500 nm

JW 1.7 Die 8 HT



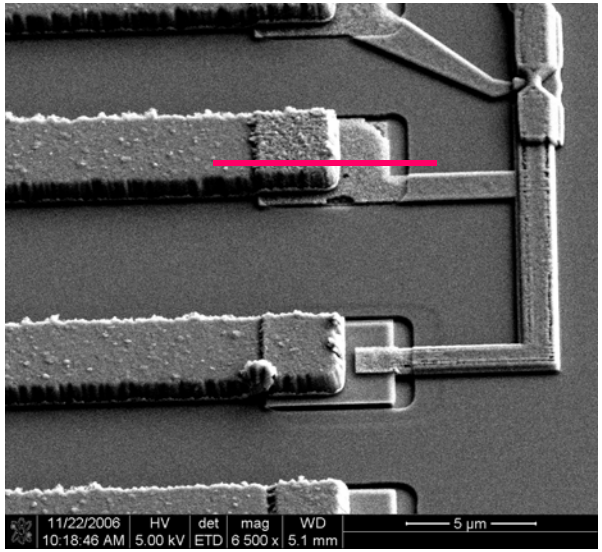
metal

LG – poly Si

LG – poly Si

SOI Si

JW 1.7 Die 8 HT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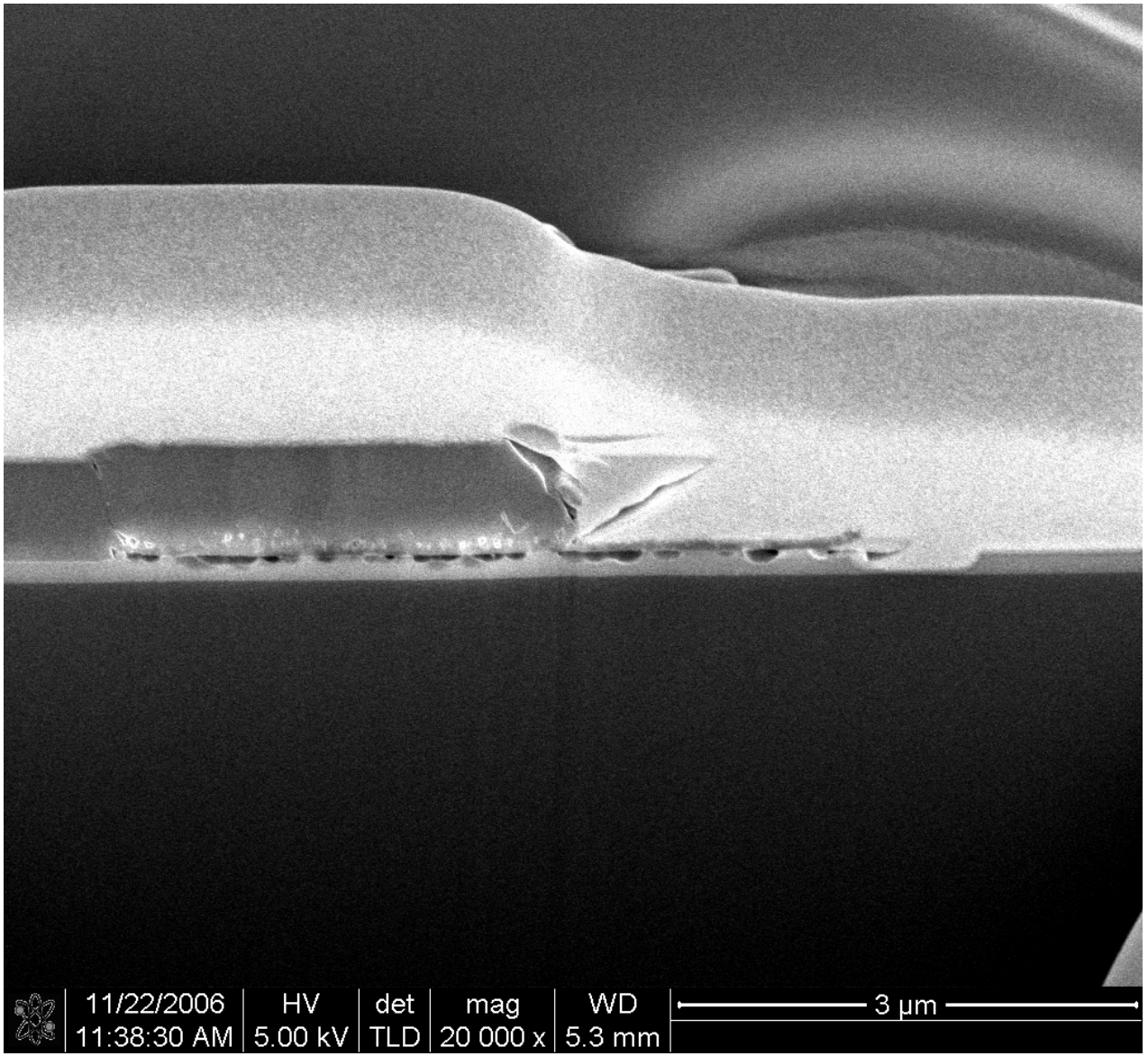
HV
5.00 kV
det
ETD
mag
6 500 x
WD
5.1 mm
5 µm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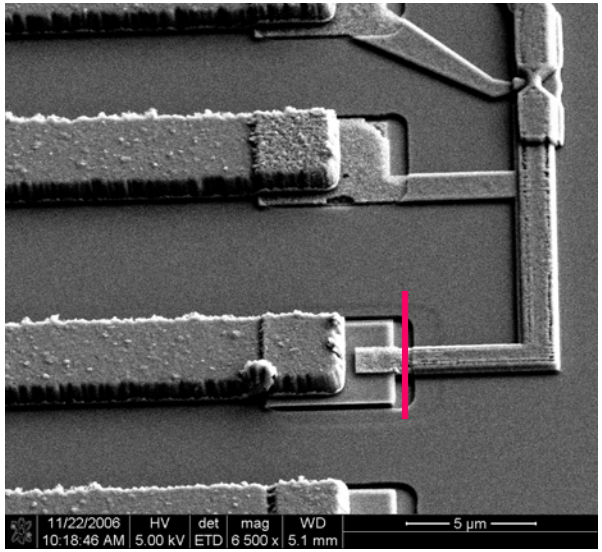
det
TLD
mag
20 000 x
WD
5.3 mm
3 µm

JW 1.7 Die 8 HT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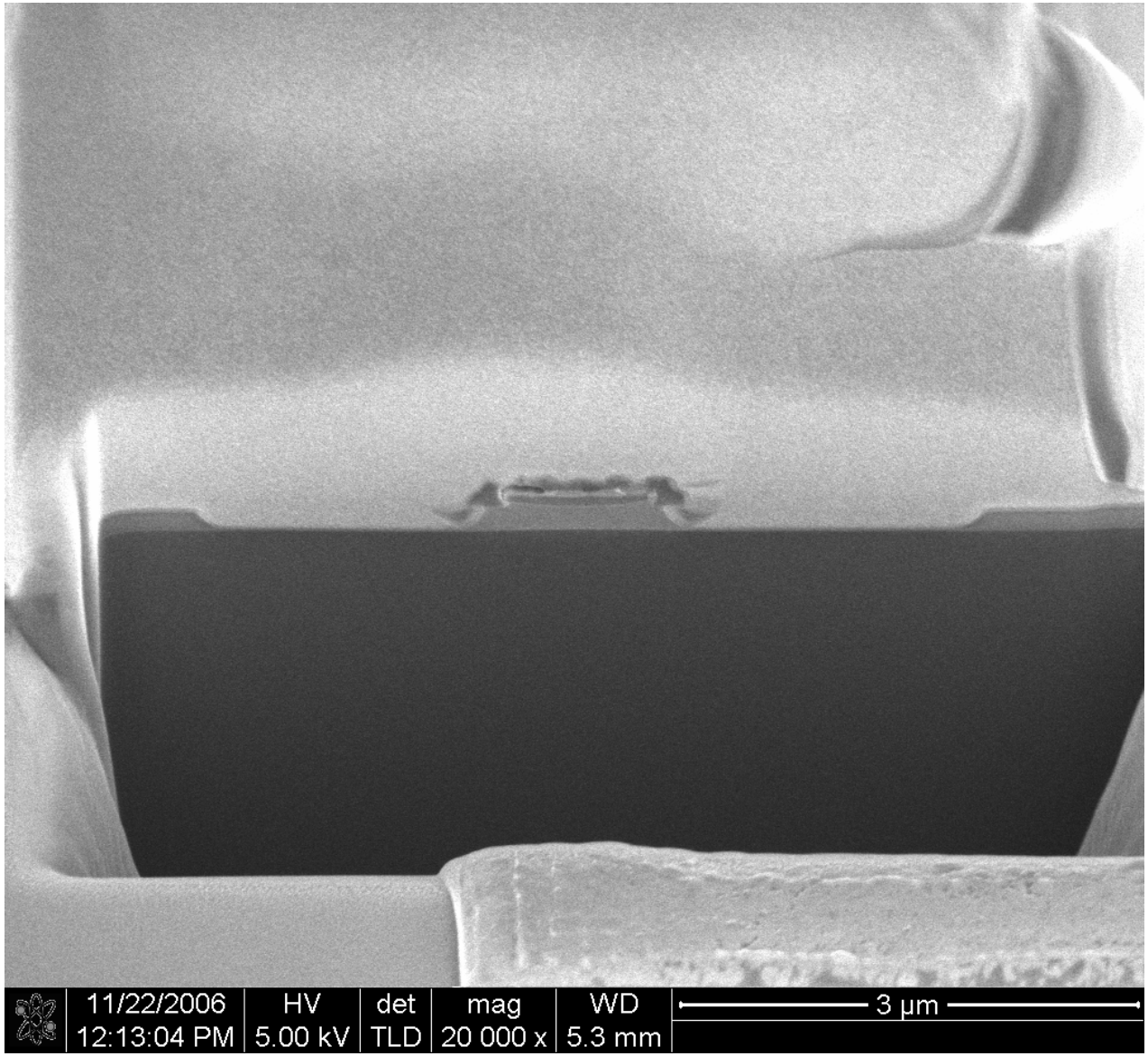
10:18:46 AM
HV
5.00 kV
det
ETD
mag
6 500 x
WD
5.1 mm
5 µm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det
TLD
mag
20 000 x
WD
5.3 mm
3 µm